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DSPs POWER THE RACE TO 4G

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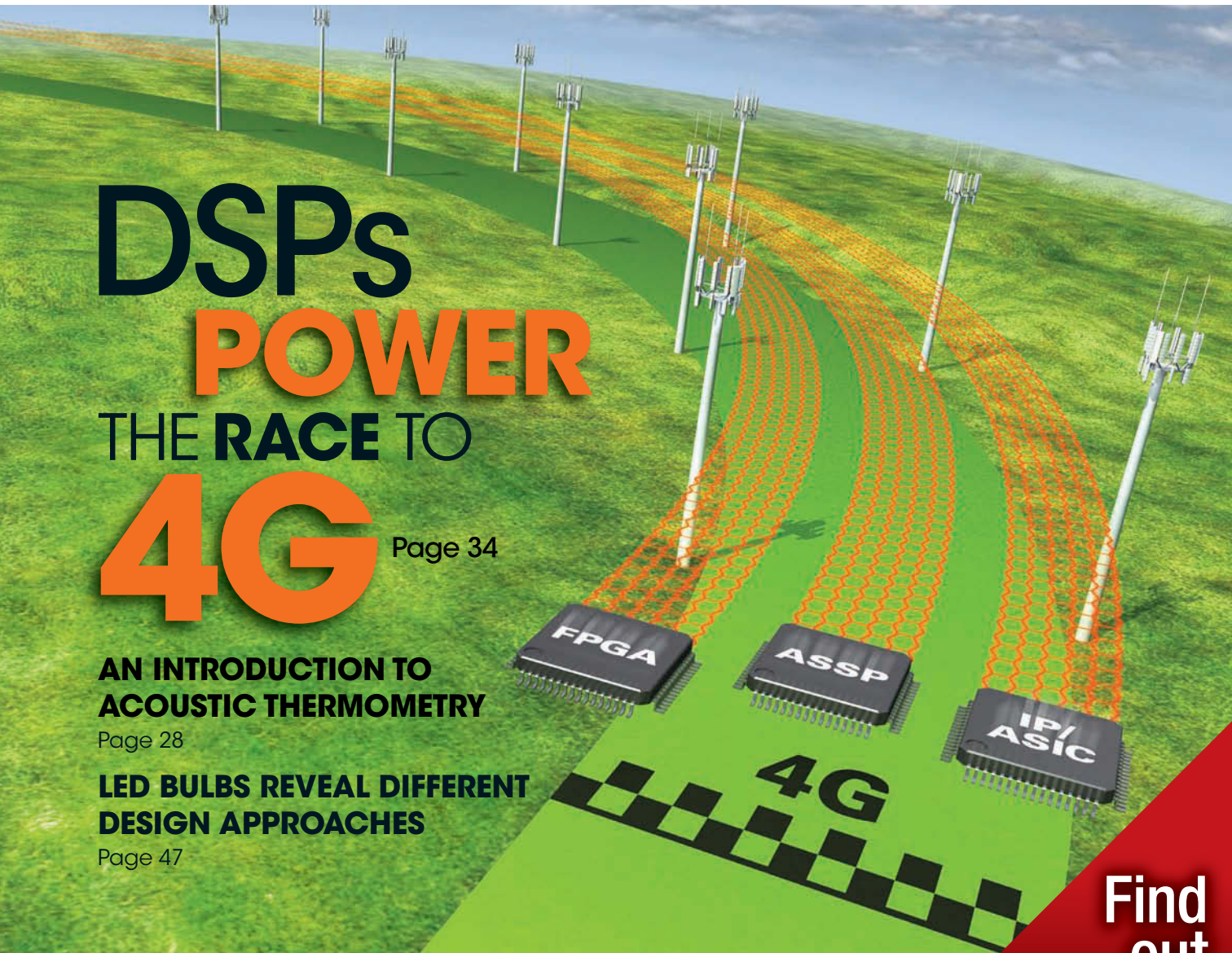

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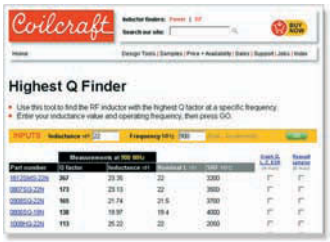

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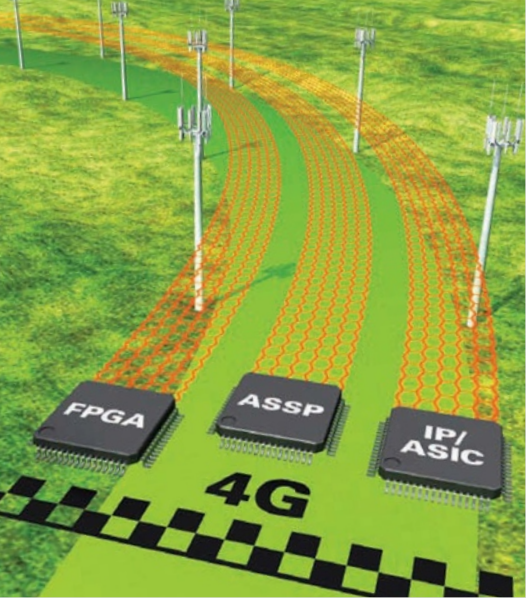

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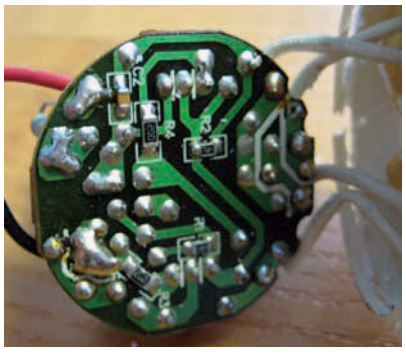
DSPs power the race to 4G

An introduction to acoustic thermometry



LED bulbs reveal different design approaches

COVER: JOHN MACNEILL

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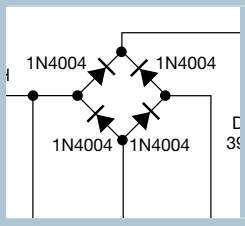
DESIGNIDEAS



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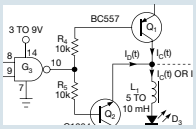

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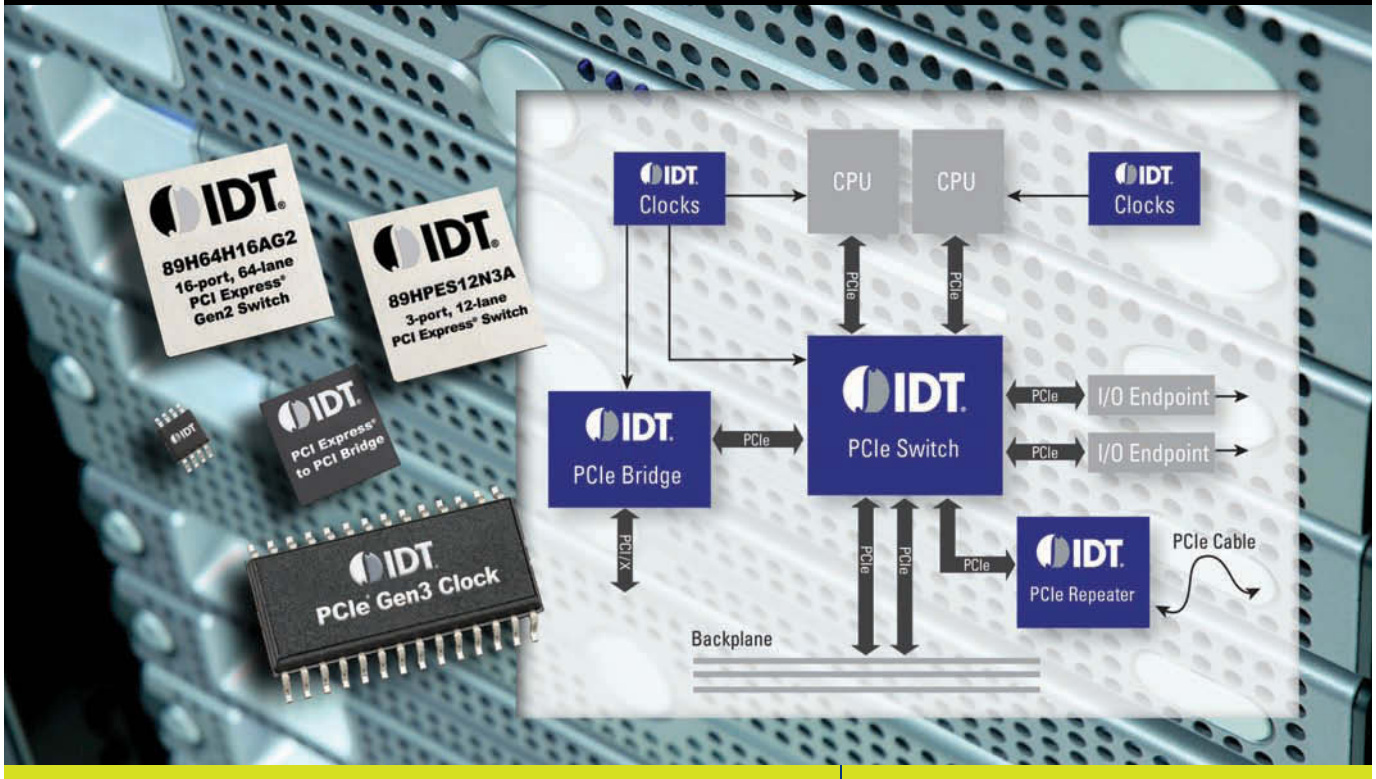

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BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

Taking network neutrality personally

I hope by now that my consistent stance on network neutrality is clear. As I wrote in June 2008, circumventing network neutrality might involve the performance degradation or a complete blockage of services, protocols, or ports. Although I understand the technical reasons that these heavy-handed measures might be attractive to network administrators, I remain concerned about the societal impacts of access limits on diverse information that these moves imply, as well as their negative impact on the free-market development of new and improved Internet services.

However, a subtler form of network neutrality could come into play if bandwidth tiers become pervasive. I wonder, for example, how closely the ISPs (Internet-service providers) will monitor how much data customers download and serve to others, the origin and destination of that data, and what the ISPs will do with that information. For example, will an ISP slap a surcharge on customers using excessive bandwidth for using the ISP's VOIP (voice-over-Internet Protocol) service? Perhaps this example is not the best because VOIP communications is a small-payload service, so consider instead videoconferencing. Will AT&T look the other way if its bandwidth-hungry customers are heavy Yahoo! Messenger video-chat users because AT&T has a business relationship with Yahoo?

Speaking of payloads, consider the biggest bandwidth user of all: video downloads. Will ISPs disregard bandwidth caps for customers of their own or their partners' movie and TV services? Conversely, what impact will bandwidth caps have on new, compelling offerings, such as Hulu and Netflix's Watch Instantly?

The network-neutrality debate will soon affect my broadband pipe, which AT&T's DSL (digital subscriber line) provides. AT&T will begin on May 2 instituting bandwidth caps of 150 Gbytes/month for copper-delivered DSL customers and 250 Gbytes/month for fiber-supplied U-verse users. Beyond that threshold, AT&T will charge $10 for incremental 50-Gbyte upstream and downstream bandwidth usage per month. Note that AT&T chose to institute bandwidth caps rather than throttle down temporary customer-specific bandwidth during heavy network-usage periods, which some other wired and wireless ISPs employ. AT&T claims that it instituted the caps because it has experienced a dramatic increase in the amount of sent and received data over its wire-line broadband networks. A small fraction of customers drove this increase; the top 2% of customers use about 20% of the network's total capacity. If network congestion were the true reason for the company's actions, however, wouldn't it instead choose to throttle back the bandwidth for heavy users?

Unlike with a shared local-loop cable-Internet topology, each DSL subscriber has a direct connection to the local exchange switch, which then connects to a regional switch through a fiber-optic tether. Network upgrades are therefore relatively straightforward and inexpensive for a carrier such as AT&T to implement, yet the company's financial statements indicate that it is forgoing them because land-line revenues are decreasing as an increasing number of former subscribers drop their POTS (plain-old-telephone-system) connections for cellular-only usage profiles. AT&T was slow to offer "naked" DSL service, which remains financially unattractive versus bundled plans, and uptake of its U-verse fiber-based services has been muted at best.

It's important for companies to be honest about the true reasons for policy changes.

AT&T reserves a percentage of the fiber bandwidth it delivers to its U-verse Internet-service customers for optional AT&T-branded VOIP and IPTV (Internet Protocol-television) services, whose use doesn't count against bandwidth caps. Conversely, if you were to use Ooma or Vonage as your VOIP provider or obtain your TV content from Hulu Plus or Netflix Watch Instantly, these bandwidth demands would accrue toward the cap thresholds. In either case, AT&T wins: It charges its customers overage fees, or it redirects them toward lucrative branded service tiers and options.

AT&T is free to institute whatever policy changes it chooses, subject to legal constraints; the market will judge whether those decisions are wise. It's important, however, for companies to be honest about the true reasons for policy changes. EDN

Contact me at brian.dipert@ubm.com.

Read an expanded version of this column in the Brian's Brain blog at www.edn.com/110421eda.

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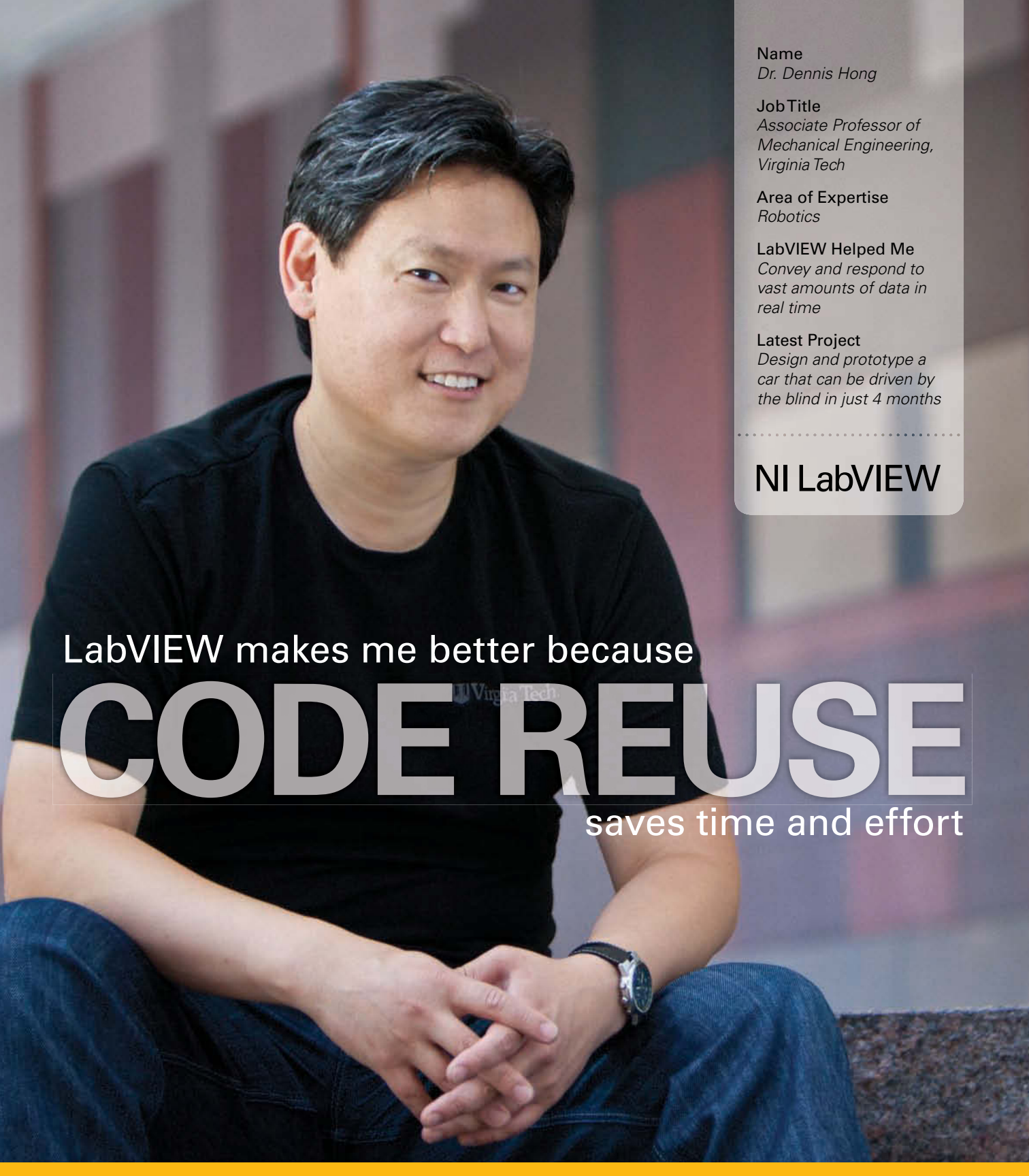

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Wireless-charging systems begin to appear in the mobile-phone market

Since last July's WPC (Wireless Power Consortium) announcement of its Qi (pronounced "chee") standard for wireless charging, hardware companies have been releasing both charging stations and device adapters. Last month, for example, Energizer (www.energizer.com) introduced both adapters and charging mats for mobile phones. The mats look like the protective case that many users purchase for their phones; hence, they are a perhaps-unnecessary expense. An iPhone-adapter sleeve and the charging mat together sell for approximately $120.

Meanwhile, LG (www.lg.com) has introduced the 6.29×3.54×0.39-in. inductive charging pad for the $70 WCP-700, which will become available this month. According to officials at Fulton Industries (www.fultonindoh.com), the creator of the eCoupled intelligent wireless-power technology that the Qi standard employs, the LG device uses hardware from Texas Instruments (www.ti.com) that provides the Qi technology for the WCP-700.

The eCoupled/Qi approach is not the only wireless-charging technology choice available. At January's CES (Consumer Electronics Show), mobile-phone chip-maker Qualcomm (www.qualcomm.com) announced that it was forming separate alliances with Duracell (www.duracell.com) and PowerMat (www.powermat.com). Qualcomm has developed WiPower, a wireless-charging technology that uses what the company terms near-field magnetic resonance to wirelessly transfer energy between a charging pad and a mobile device. WiPower can work at greater distances than the Qi standard. Powermat has its own wireless-charging technology, and Duracell has introduced MyGrid, which the company based on technology it licensed from WildCharge (www.uk.wildcharge.com).

All of these approaches are much more expensive and less energy-efficient than using a wired "wall wart," but several companies clearly see a demand for wireless charging due to the "coolness factor" and ease of use. (For a summary of the pros and cons, see "Industry consortium releases Qi wireless standard," *EDN*, July 28, 2010, http://bit.ly/fe3rD6). **—by Margery Conner**

▷**Wireless Power Consortium**, www.wirelesspowerconsortium.com.

TALKBACK

"It happens that the mil spec for 'good' and 'bad' RTV [room-temperature-vulcanizing sealant] transposed the same numbers! And with a little dyslexia anyone can confuse the two."

—Design and manufacturing engineer Geoffrey Campbell, in *EDN*'s Talkback section, at http://bit.ly/ffsn59. Add your comments.

The Energizer charging mats look like the protective case that many users purchase for their phones; hence, they are a perhaps-unnecessary expense. An iPhone-adapter sleeve and the charging mat together sell for approximately $120.

Researchers build room-temperature spintronic computers

Researchers at the University of Utah have built spintronic transistors to align the magnetic spins of electrons for a record period of time in silicon chips at room temperature (**Reference 1**). "Electronic devices mostly use the charge of the electrons, a negative charge that is moving," says Ashutosh Tiwari, an associate professor of materials science and engineering at the university. "Spintronic devices will use both the charge and the spin of the electrons. With spintronics, we want smaller, faster, and more power-efficient computers and other devices."

In the National Science Foundation (www.nsf.gov)-funded study, researchers used electricity and magnetic fields to inject spin-polarized carriers—electrons with their spins aligned either all up or all down—into silicon at room temperature. The researchers used magnesium oxide as a tunnel barrier to get the aligned electron spins to travel from one nickel-iron electrode through the silicon semiconductor to another nickel-iron electrode.

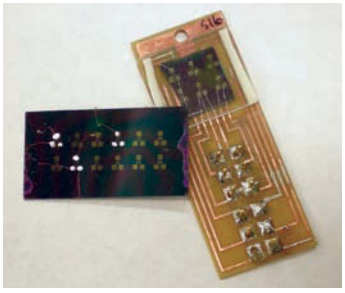
Without the magnesium oxide, the spins would get randomized almost immediately, with half up and half down, explains Nathan Gray, a doctoral student at the university. "Almost every electronic device has silicon-based transistors in it," says Gray. "The current thrust of the industry has been to make those transistors smaller and to add more of them into the same device" to process more data. "Instead of just making transistors smaller and adding more of them, we make the transistors do more work at the same size because they have two ways [electron charge and spin] to manipulate and process data," he adds.

Much of the previous research on spintronic transistors involved using optical radiation in the form of polarized light from lasers to orient the electron spins in nonsilicon materials, such as gallium arsenide and organic semiconductors, at very low temperatures. "Optical methods cannot do that [orientation] with silicon, which is the workhorse of the semiconductor and electronics industry, and the industry doesn't want to retool for another material," says Tiwari. "Spintronics will become useful only if we use silicon."

Tiwari points out that researchers of earlier studies had to cool most of the devices to very low temperatures. Previous experiments have focused on temperatures colder than –200°F to align the electrons' spins either all up or all down. The researchers' method of putting spin inside the silicon requires no cooling.

The experiment used a flat piece of silicon measuring about 1×0.3×1/50 in. The researchers deposited an ultrathin layer of magnesium oxide and a dozen transistors on the silicon wafer so they could use the transistors to inject electrons with aligned spins into the silicon and later detect them. Each nickel-iron transistor had three contacts or electrodes: one through which researchers inject electrons with aligned spins into the silicon and detect them, a negative electrode, and a positive electrode to measure voltage. The researchers send direct current through the spin-injector electrode and negative electrode of each transistor. Keeping the current steady, the researchers measure variations in voltage while applying a magnetic field to the apparatus.

"By looking at the change in the voltage when we apply a magnetic field, we can find how much spin has been injected and the spin lifetime," says Tiwari. The electrons retained their spins for 276 psec. Using that data, the researchers calculate the spin-aligned electrons' diffusion length at 328 nm.



A dozen three-contact nickel-iron transistors sit on a silicon chip coated with an ultrathin film of magnesium oxide (left). A six-transistor chip (right) attaches to electrical contacts for experiments showing that the magnetic spins of electrons can align as they travel through silicon at room temperature (courtesy Jiajia Tan, University of Utah).

"It's a tiny distance for us, but, in transistor technology, it is huge," says Gray. "Transistors are so small today that [that distance is] more than enough to get the electron where we need it to go." The use of electronic spin injection is more practical than using optical methods such as lasers, he adds, because lasers are too big for chips in consumer-electronics devices. Spintronic-computer processors also require less power than electronic devices, so a battery that may power an electronic computer for eight hours might last more than 24 hours on a spintronic computer.

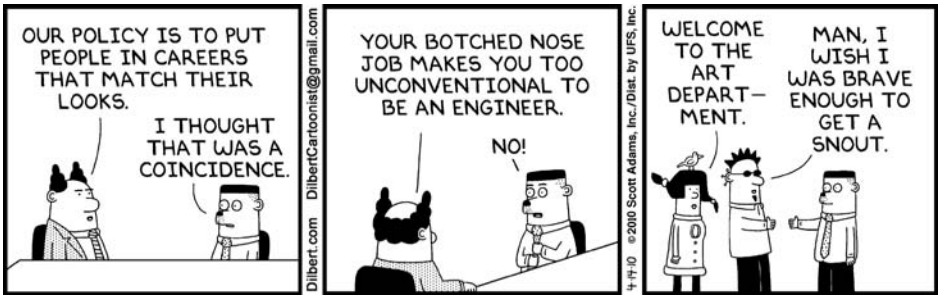
—by Suzanne Deffree

University of Utah, Department of Materials Science and Engineering, www.mse.utah.edu.

REFERENCE

Gray, Nathan W, and Ashutosh Tiwari, "Room temperature electrical injection and detection of spin polarized carriers in silicon using MgO tunnel barrier," *Applied Physics Letters*, Volume 98, Issue 10, March 10, 2011, http://bit.ly/dV3oZp.

DILBERT By Scott Adams



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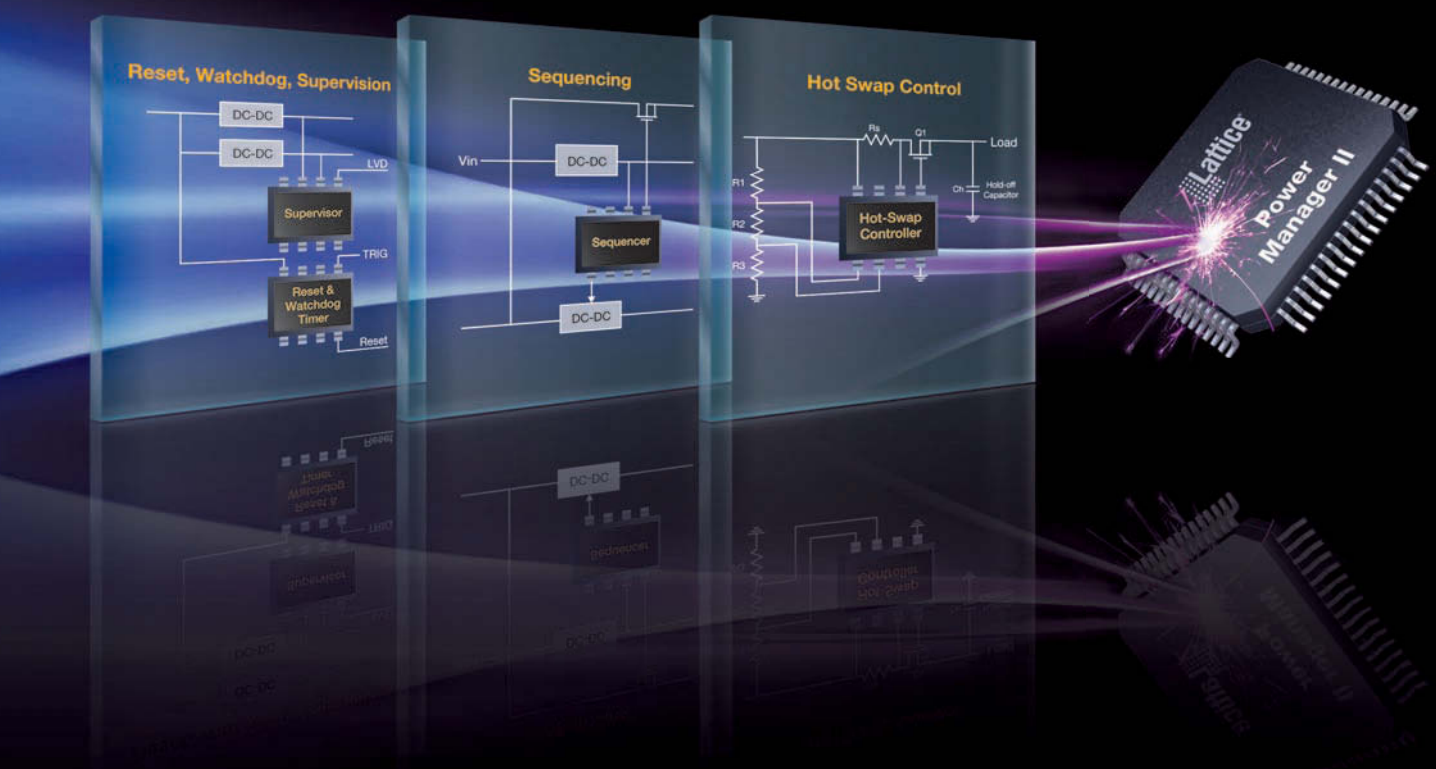

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Modular logic analyzer meets high-performance-memory-bus test requirements

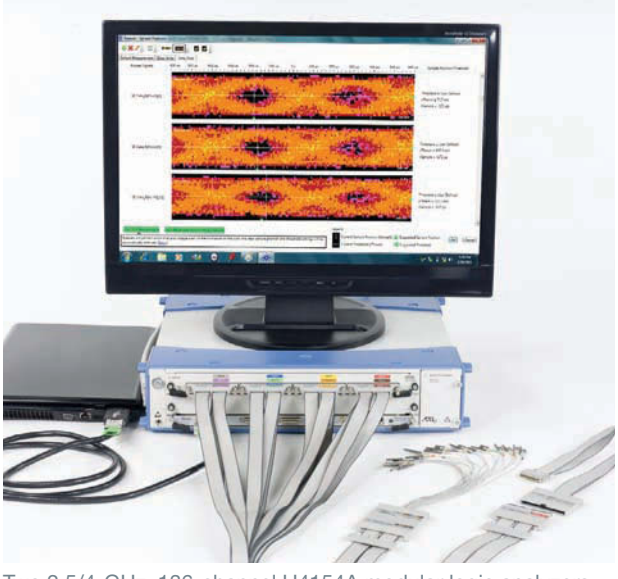
Serial-bus architectures have been unable to make inroads into parallel buses' turf in some important applications, including high-speed memory. With the exception of the FBDIMM (fully buffered dual-in-line memory-module) bus, all DDR buses continue to be parallel structures. Although they are narrower than parallel buses that provide equal throughput, serial buses dissipate more power and thus more heat, a counter-intuitive finding that will surely surprise many people. As the history of the DDR3 bus indicates, this situation shows no signs of changing for at least a few years, and the industry is mounting a major effort to further increase the speed of parallel DDR buses. Successive iterations of DDR3 have enabled data rates to increase to more than 2 Gbps/channel today from 800 Mbps/channel in 2006, and a new and even faster generation of memory buses, DDR4, is on the horizon.

In today's memory buses, 64-bit-wide structures are common. In such cases, 64 bits refers only to the lines that carry data; the complete bus also includes multiple clock and strobe lines, so total bus widths of 128 bits and more are not unusual. The tool of choice for debugging such buses has been the logic analyzer, but logic analyzers have failed to keep pace with high-speed-memory performance. To address this problem, Agilent recently announced a suite of hardware and software products. The U4154A modular logic analyzer offers 12.5-GHz timing zoom and performs state analysis at 4 Gbps/channel on 68 channels and at 2.5 Gbps/channel on 136 channels. The M9502A chassis, which can accommodate two U4154As, includes two AXIe (Advanced Telecommunications Computing Architecture Express Extensions for Instrumentation) slots. The B4622A protocol-compliance and analysis software tool enables automated measurements on deep DDR-bus traces to quickly identify protocol problems and provide an overview of system performance. The company's proprietary EyeScan technology enables the logic analyzer to display multichannel eye diagrams in several orders of magnitude less time than an oscilloscope could.

In measurements on new memory buses, voltage and timing resolution are key attributes because the buses achieve their high throughput by reducing both the duration of a unit interval and the voltage difference between the high and the low logic states. According to Agilent, although high-performance scopes provide better resolution, the logic-analyzer-based system, which can position samples within 5 psec and 5 mV, delivers adequate time and voltage resolution for nearly all applications and is by far the industry's fastest tool for obtaining multichannel eye diagrams from high-performance memory buses. Prices for the U4154A start at $115,000 for a 136-channel, 2.5-GHz system, including an analyzer module, a chassis, and probe cables. Probes are additional.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/logic, www.agilent.com/find/modular.



Two 2.5/4-GHz, 136-channel U4154A modular logic analyzers can fit into the low-profile, two-slot M9502A AXIe chassis. The small black unit to the left of the chassis is the user-supplied PC that controls the system.

TVS-DIODE ARRAY ADDRESSES USB 3.0 SIGNAL-INTEGRITY ISSUES

04.21.11

Littelfuse's new SPA (silicon-protection-array) SP3011 TVS (transient-voltage-suppression)-diode array addresses the signal-integrity issues of USB (Universal Serial Bus) 3.0 protection. The six-channel array provides ESD (electrostatic-discharge) and low-level-voltage-transient protection without compromising signal integrity on high-speed USB 3.0 ports. One member of the series, the SP3011-06UTG, has a parasitic capacitance of 0.4 pF, which minimizes signal degradation on four 5-Gbps and two 480-Mbps data lines. Each channel provides ±8-kV contact-discharge ESD protection, the maximum level, according to IEC61000-4-2. The device has 6V standoff voltage, 0.5-µA leakage current, and 8-kV ESD-contact voltage. The array, in split-reel quantities, sells for 68 cents to $1.20.

—by Margery Conner

▶**Littelfuse, www.littelfuse.com.**

The SP3011 TVS-diode array targets signal-integrity issues in USB 3.0 protection.

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

A Foolish Question about Op Amps and Capacitors

Q: Can you help with the strange interaction between the op amp and capacitors in my circuit?

A: This sounded more like a Frequently Asked Question than a Rarely Asked Question, but turned out to be neither.

Interaction between op amps and capacitors goes back to the beginning of op amp time, with three classic problems occurring most frequently. I tried to narrow down the specific problem this customer was facing, figuring that it should only take a few minutes to solve… boy was I wrong.

The first classic problem in the study of op amp stability involves capacitance on the inverting input, and arises due to the interaction of the feedback resistor with the combined op amp input capacitance and parasitic capacitance at the inverting input. The capacitance and feedback resistor introduce a pole in the feedback response that can lead to decreased phase margin and instability. "No, no," he said, "It's something else." "Alright," I said, "No problem; let's move forward."

Output load capacitance was my next stop; capacitance found at the output can cause overshoot, ringing, and stability issues. The op amp output impedance and the load capacitance form a pole that alters the op amp transfer function and reduces phase margin, which leads to ringing and overshoot. "No, that's not it either," he said.

He finally said that it appeared to be an issue with the bypass capacitors (the third classical problem). I started to launch into my standard litany on bypass capacitors when he stopped me. "This is no ordinary bypass capacitor issue," he cautioned, "It's something different." When he turned the power supplies off, the bypass capacitors stayed charged, and the op amp continued to deliver an output voltage. "That's perfectly common," I told him, "The output voltage will last until the bypass capacitors are discharged, but will go away in a few nanoseconds." "No," he said, "the capacitors never discharge." He'd wrestled with this problem for months now. He hadn't applied power to the circuit for over a month, but the capacitors were still charged and the circuit was still working! How could this be? Even a micropower device should have bled off the stored charge by now. When I asked him what type of capacitors he was using; he laughed and said, "Flux capacitors[1], of course!" April Fools!

[1] The Flux Capacitor is featured in "Back to the Future," a 1985 Universal Pictures movie in which a single Flux capacitor provided 1.2 Gigawatts of power, enough to enable time travel in the movie!

To Learn More About Op Amp Stability
http://dn.hotims.com/34930-100

Contributing Writer John Ardizzoni is a Senior Application Engineer at Analog Devices in the High Speed Linear group. John joined Analog Devices in 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 30 years experience in the electronics industry.

Have a question involving a perplexing or unusual analog problem? Submit your question to: www.analog.com/askjohn

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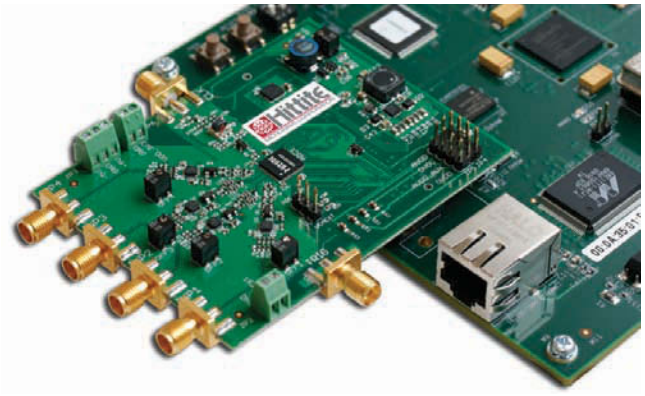
Quad-interleaved, 640M-sample/sec, 12-bit ADC has 14-bit mode

Each converter in Hittite Microwave's new 12-bit, 640M-sample/sec, quad-interleaved HMCAD1520 ADC operates at 160M samples/sec. The part targets applications in test-and-measurement equipment, diversity receivers, and ultrasound devices. Limiting the device to 105M samples/sec causes it to operate in precision mode and deliver 14-bit outputs. The device has four 160M-sample/sec converter inputs and outputs, as well as internal interleave controls so that you can make the IC serve as a 640M-sample/sec part. An integrated cross-point switch that precedes the four converters can route any of the inputs to any of the four internal converters. In interleaved, 640M-sample/sec mode, the ADC has an ENOB (effective numbers of bits) of 10. The ENOB falls to 8 with a gain of 10. The ENOB is 10.8 in 160M-sample/sec mode and 11.8 in precision mode. The SNR (signal-to-noise ratio) is 70 dB, and SFDR (spurious-free dynamic range) is 65 dB. SNR rises to 74.5 dB in the 14-bit precision mode, and SFDR is 85 dB with a 70-MHz input bandwidth.



The evaluation board for Hittite's HMCAD1520 ADC allows you to assess the unit's performance.

The HMCAD1520 operates from a 1.8V supply and accepts CMOS-logic-level-control inputs of 1.7 to 3.6V. Power dissipation is 490 mW at 640M samples/sec and 603 mW in precision mode. You can put the device in idle mode with one pin, and you can power down each channel through the SPI (serial-peripheral interface). The unit wakes up from sleep mode in 0.5 µsec and from power-down mode in 15 µsec.

The ADC has an internal reference, fine and coarse gain control, and internal offset-voltage correction for each channel. Each of the four converters has a dedicated LVDS (low-voltage-differential-signaling) output pair. You can configure these outputs for 12-, 14-, 16-, or dual 8-bit formats. An internal, low-jitter, programmable clock divider enables the use of one clock source for all operational modes. The ADC outputs LVDS data- and frame-synchronization clocks for data capture at the receiver.

The HMCAD1520 comes in a 48-pin, 7×7-mm QFN package, operates from –40 to +85°C, and sells for $65.75 (500). An evaluation board is available for $925. **—by Paul Rako**

▷**Hittite Microwave**, www.hittite.com.

Solid-state drives: lower SATA speeds but more advanced lithographies

Intel recently unveiled its 320 series, which employs a 25-nm, 2-bit-per-cell, MLC (multilevel-cell)-NAND-flash-compatible Intel storage controller. Cost and capacity are the primary beneficiaries of this process and processor transition. Intel has added 300- and 600-Gbyte product tiers to its earlier-generation 2.5-in.-form-factor X25-M products. The 320 series also comes in a 1.8-in. form factor in 80-, 160-, and 300-Gbyte flavors. However, the Intel-proprietary controller is not yet 6-Gbps SATA (Serial Advanced Technology Attachment)-compatible, although it supports SATA II features, such as native-command queuing.

A solid-state-storage retrofit can deliver notable improvements in performance, power consumption, reliability, ruggedness, and operating noise versus that same system initially based on a hard-disk drive. When using a 3-Gbps SATA bus, which has an installed base of more than 1 billion units, the 320 series devices outperform the X18-M, the X25-M, the mini-SATA-derived 310 series, and the Marvell (www.marvell.com)-powered 510 series.

The 320 series also includes 128-bit AES (Advanced Encryption Standard) support and ATA (Advanced Technology Attachment)-password-protection cognizance. Typical active and idle power consumption are 150 and 100 mW, respectively, across the products' 0 to 70°C specified operating-temperature range. Integrated capacitors can fuel the drive in looming system-power-loss situations long enough to enable the controller to transfer queued information from the RAM buffers to the nonvolatile NAND-flash-memory array.

The device also has a 1.2 million-hour MTBF (mean time between failures) and one sector per 10^{16} bits read UBER (uncorrectable-bit-error rate). Intel has further beefed up the X25-M drives' already-formidable error-detection and -correction facilities with both redundant flash-memory capacity and controller hardware and software intelligence to sense and appropriately respond to pending storage failures. Intel claims that the drives can compensate for the demise of an entire flash-memory die.

The 40-, 80-, 120-, 160-, 300-, and 600-Gbyte versions of the 320 series sell for $89, $159, $209, $289, $529, and $1069 (1000), respectively, in a 2.5-in. form factor.—by Brian Dipert

▶**Intel Corp, www.intel.com.**

INNOVATORS

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VOICES

Dag Spicer: saving the artifacts of the information age

Dag Spicer is senior curator at the Computer History Museum (Mountain View, CA), where he has worked since 1996. Spicer recently discussed his mission with *EDN*, including the conception and design of exhibitions and projects and writing and consulting on computer history. An excerpt of that interview follows. For the full version, go to www.edn.com/110421pa.

How did you come to be a curator at the Computer History Museum?

A I've always been an electronics hobbyist, but when university came along I went into history. After a couple of years, I realized that I really wanted to be an engineer, so I went to UBC [University of British Columbia] and did an EE. I worked in the industry for six or seven years and then went back to school to finish the history degree. Then I did a master's in the history of technology.

Didn't the museum start in Massachusetts [where Gordon Bell worked for Digital Equipment Corp]?

A Yes, we moved the collection here in 1996. The Boston museum had changed into a science center for kids. It had an amazing collection of pioneering computers, but they were never being seen. The center of gravity changed from Route 128 to Silicon Valley after the minicomputer era ended.

What is now the museum's mission?

A Our mission formally is to preserve and present the artifacts and stories of the information age. There are more than 100,000 objects, including more than a linear mile of paper.

Does the paper include old punch tapes?

A Oh, the software collection is another collection. That [collection] has unique challenges. One: Can you read the medium—a floppy disk, say? Two: Do you have the software that knows what the bytes mean? Three: Do you have the right environment, hardware, processor, and operating system? We have a software curator who handles all those details.

What is the oldest working computer that you have at the museum?

A Most of the computers are not working because they have huge air-conditioning or power requirements, or, in some cases, we've lost the recipe. We have three functioning computer systems: the 1401, a 1951 IBM medium-scale mainframe. You can punch cards, run them, and get a printout. Then there's the 1620, an IBM scientific and engineering computer that came out in about 1961. And there's the

DEC [Digital Equipment Corp] PDP-1.

How do you acquire your collections?

A Most of it comes from individuals; very little comes from companies. For most tech companies, the past is not something to be cherished or learned from; it's to be quickly forgotten. They are also worried about IP [intellectual property], even if the technology is 30 years old.

How do you get software for your collection?

A It's been difficult. We managed to get it for MacPaint, but it took a friend of [Apple Co-Founder and Chief Executive Officer] Steve Jobs to talk to Jobs directly. Lawyers worry: Is there something still in the old code? Our software SIG [Special Interest Group] views software as poetry—as an elegant human-created work.

Do you also have a semiconductor SIG?

A We've had fantastic donations in the semiconductor space. [Semiconductor consultant] Doug Fairbairn, who was at Xerox PARC [Palo Alto Research Center], is in our semiconductor SIG. We have one of the first seed crystals, from Fairchild, from a silicon ingot that literally started Silicon Valley.

How do you make the exhibits appeal to the general public?

A It's based on milestones; it's not encyclopedic. When you go through the exhibit you hear the museum's voice. The voices of the museum explain history to you. Each gallery has a PVS [personal video station], which is a touchscreen that contains footage of the actual creators of the thing you are looking at. So you can hear [former IBM fellow and Amdahl Corp Founder] Gene Amdahl and [IBM developer] Fred Brooks talk about the IBM 360.

You also have a storage SIG?

A Yes, a lot of people don't know that hard disks have actually exceeded Moore's Law in rate of density increase. It's as much an enabling technology for the PC as microprocessors are.

Tell me about the oral-history project.

A One of the great things about the museum is that most of these people are still alive. We're not like an art museum showing da Vinci, where you have no idea what he was thinking. We have more than 450 oral histories, and the transcripts are online.

Is there anything else you would like to mention?

A I would point out that we have the best collection in the world of computing equipment, and it is largely due to Bell and his wife, Gwen. Because of their foresight, these items are now well-preserved at the museum.

—interview conducted and edited by Mike Demler


INNOVATORS
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BY BONNIE BAKER

A little electrical overstress won't hurt, right?

Thermal overstress with a transformer or metallization damage at the bond-wire junction of an IC can cause IC EOS (electrical overstress), which in turn can create an electrical short. An EOS event also can compromise the integrity of the IC's ESD (electrostatic-discharge) circuitry. In this case, the voltage exposure to an IC's input or output pin is well below the voltage and well above the exposure time of an ESD event.

A forward-voltage spike that exceeds a device's absolute maximum ratings will cause an EOS event or at least accelerate the IC's oxide-defect failures. In the worst case, this overvoltage-stress, or EOS, event will damage the IC circuit—usually, the ESD cells near the pin pad (**Figure 1**).

In **Figure 2a**, the operational-amplifier macromodel, which Texas Instruments' TINA software tool generated, shows a simple follower circuit using a low-power OPA364 CMOS op amp. V_{G1} is a low-frequency signal from a transducer output. The transducer resides at a distance from the amplifier, and a cable, TL_1, connects the transducer to the op amp's noninverting input. The surrounding environment injects a transient signal, V_{G2}, on the cable. V_{G2} combines with the transducer's output signal, V_{G1}. The amplitude of this summed signal exceeds the maximum specified input range of the amplifier. A large transient signal triggers the op amp's input-ESD circuit.

Placing a resistor in front of this amplifier's noninverting input limits the magnitude of the damaging input current. ESD cells safely conduct amperes of current for no more than tens to hundreds of nanoseconds. When ESD cells activate during an EOS event, the duration of current conduction is usually longer than the ESD event. These same ESD cells can often continuously handle 5 to 10 mA (**Figure 2b**). An overvoltage signal may affect them, or they may be completely safe. In either case, it is worth the effort to evaluate potential problems with your circuit.

If IC components operate beyond their safe operating ranges, soft errors or permanent damage can occur. The EOS events include the occurrence of voltage or current surges during operation. Direct effects include IC-junction damage, metallization damage, or charring of the device. EDN

Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.

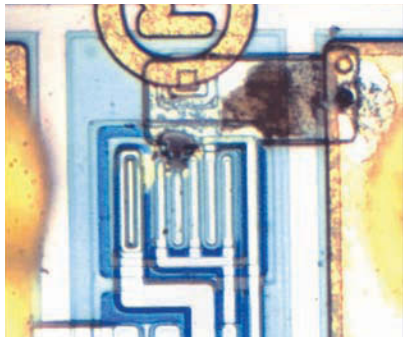
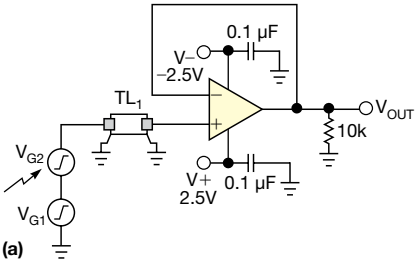


Figure 1 In the worst case, an overvoltage-stress, or EOS, event will damage the IC circuit—usually, the ESD cells near the pin pad.



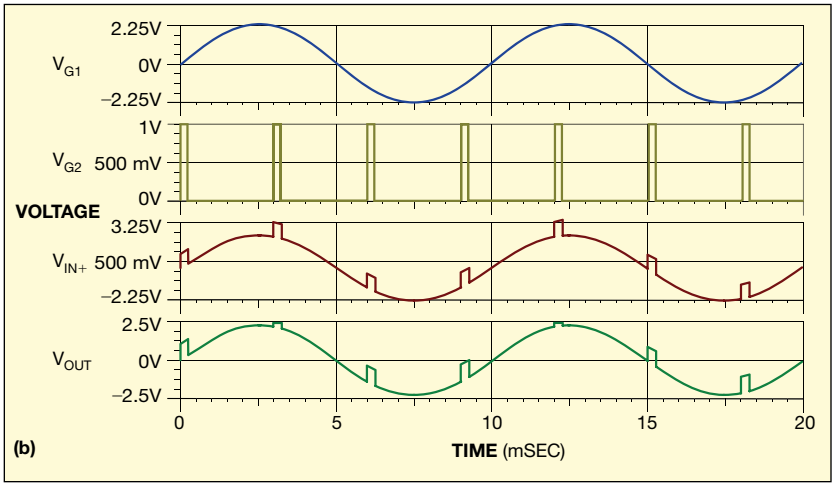


Figure 2 The operational-amplifier macromodel shows a simple follower circuit using a low-power OPA364 CMOS op amp (a). When ESD cells activate during an EOS event, the duration of current conduction is usually longer than the ESD event (b).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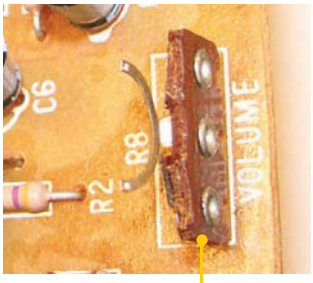
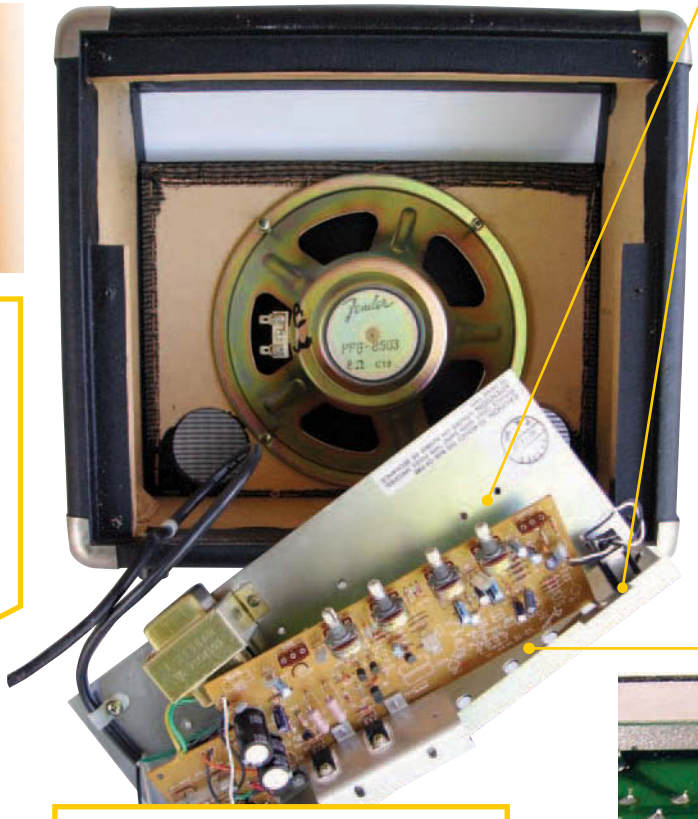
The 15W Fender Squier guitar amplifier

A friend gave me a Fender Squier guitar amplifier when he retired. The sound was terrible, and all the potentiometers made scratchy noises. I was able to pry into the vinyl-covered chip-board enclosure using only a Phillips-head screwdriver. By looking at the product photos on the Digi-Key site, I saw that the potentiometers were similar to those in the Bourns PDB181 series. Digi-Key had none in stock, but Mouser did. The company even had the "-A" audio taper for the volume. After disassembling the amp, I fired it up. Although it sounded weak, the scratchy noises were gone. After reassembling the unit, though, I found that the sound had become a tinny buzz. I again pulled the unit apart. I thought I had blown the output transistors. When they checked out OK, I noticed that the sound on the input jack seemed intermittent. I applied DeoxIT contact cleaner to the contacts and restripped and resoldered the wires between the jack and the board. Finally, I noticed that a slight pressure on the PCB (printed-circuit board) made the sound cut in and out, meaning that I had done a bad job on soldering the joint on the gain potentiometer. Once I fixed that problem, the weak volume and buzzy noises disappeared.



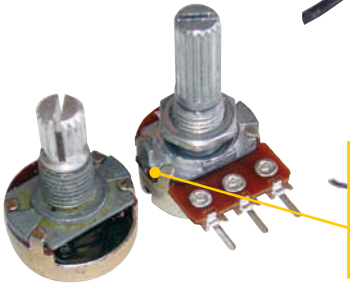
I found that two of the potentiometers were broken in half and the rest were scratchy and intermittent—not good. I replaced the no-name cheapos with genuine Bourns units. You can see, feel, and hear the quality improvement.



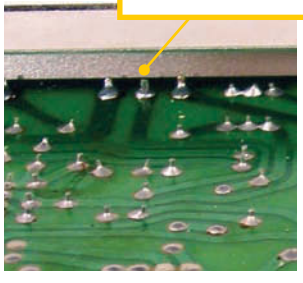
The carry-strap screws secure the chassis inside the chip-board enclosure. Two tabs secure the lower part of the panel.

One of the common mistakes mechanical engineers make is using electrical components to carry structural loads. The potentiometers should not have to support the whole PCB.

Thanks to my poor soldering job, I had to yet again pry the PCB apart to find out why the sound was intermittent.



I had to cut down the shaft and grind off the antirotation lug on the replacement potentiometer on the right.



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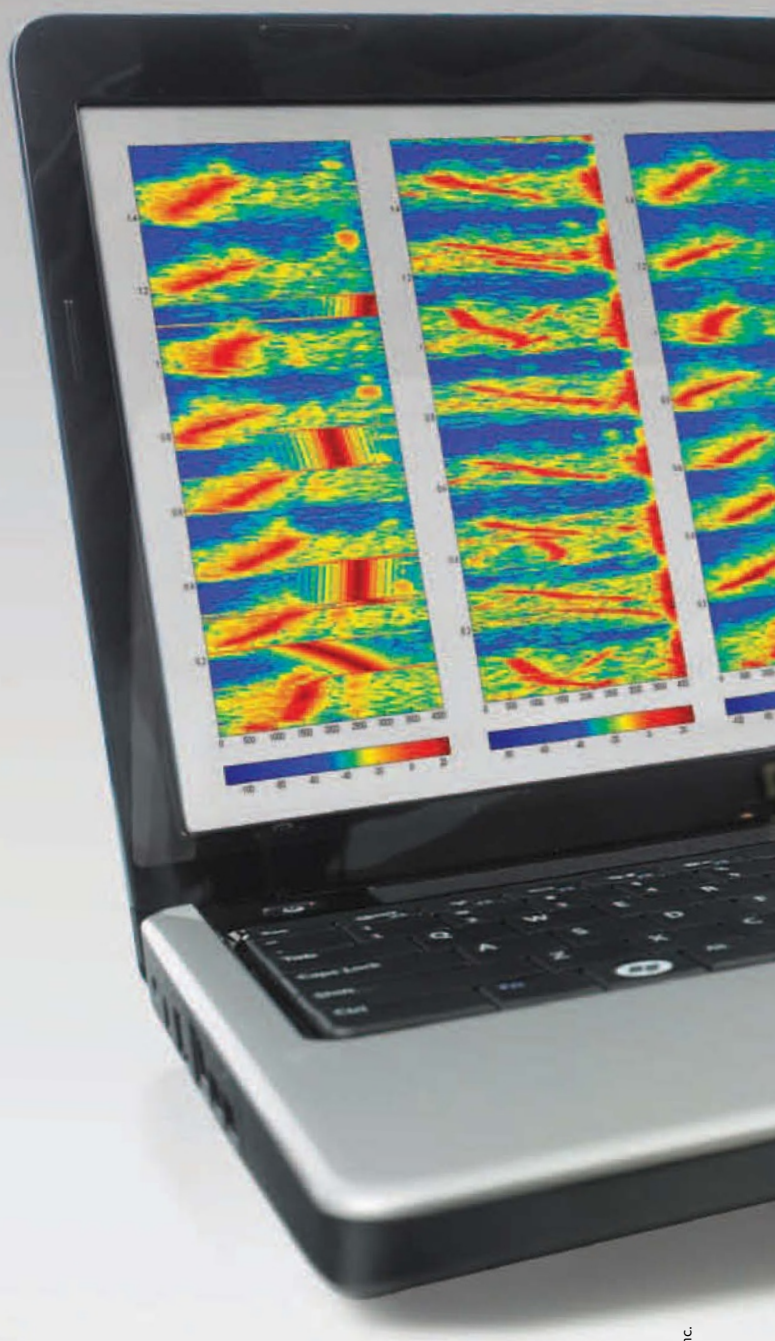

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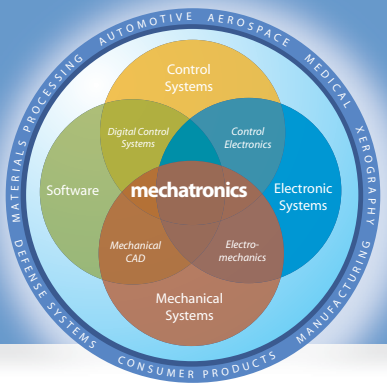

Take engineering education in context

Engineers practice engineering in context, so why do educators teach it out of context?

If a boy wants to become a baseball player, he must be able to field, throw, run the bases, and hit with power, and he must be able to apply all these skills in a game. To achieve this goal, he learns all these skills at once, improving gradually in each one while playing games, and, over time, he develops into a baseball player. The result is not only the sum of the skills he learned but also a sense of confidence and savvy that makes him a winner.

In mechatronics, the necessary skills include modeling and analysis of multidisciplinary dynamic systems, analog- and digital-control systems, and sensors and actuators with the necessary electronics. Theory and practice must be in balance when an engineer masters these skills. Putting together these skills to create a system to solve a problem rarely happens in engineering education, and, if it does, it happens for only a few students who aggressively seek out that integrated, total experience. Universities devote separate courses to each skill and somehow think that learning each skill well will magically enable a student to graduate and critically think, integrate it all, and solve a real-world problem. In the baseball analogy, this scenario would be utter madness, yet it is routine in engineering education.

I am now teaching a course in electromechanical engineering systems to 60 second-year engineers with whom I have 16 personal-contact hours each week—10 in studios and six in classes. I have no teaching assistants, just graders, and I do everything in the context of real-world engineering practice and problem solving.

The process works as follows, and the students apply and learn mathematics and physics when necessary. First, the students choose an electrical, mechanical, or electromechanical engineering system that must behave dynamically in a specified way. The students then physically model the system with simplifying assumptions and then mathematically model the system by applying the laws of nature and appropriate component-constitutive equations to the physical model. They start with a system whose model is first-order and study it from both the time- and the frequency-domain perspectives. Putting the mathematical model in a standard form—that is, time constant and steady-state gain—allows the engineers to relate performance, including speed of response, steady-state error, and relative stability, to the hardware parameters in the physical model. In some cases, the system cannot meet performance specifications while operating open loop. The students must then design and implement a feedback-control system. Closed-loop PI (proportional-integral) control of a first-order model results in a closed-loop differential equation that is second-order with a numerator of zero. I introduce second-order dynamic systems as part of the process, along with the effect that a real zero has on ideal second-order behavior, again emphasizing time- and frequency-domain perspectives.

Kevin C Craig, PhD, is the Robert C Greenheck chair in engineering design and a professor of mechanical engineering, College of Engineering, Marquette University. For more mechatronic news, visit mechatronicszone.com.

Once the students select PI-control gains by a combination of pole placement and simulation iteration, it is time to build the system. First, the students build an analog-op-amp system with a difference amplifier and PI controller. They must then address loading effects and the limit on the control effort due to op-amp implementation, as well as compare measurements to model predictions and adjust the model. The inexpensive and open-source Arduino microcontroller is used for digital control, with the MathWorks Matlab/Simulink Real-Time Workshop providing automatic code generation. Students can address issues such as pulse-width modulation; lowpass filtering, which introduces a real pole; saturation; and analog-to-digital and digital-to-analog resolution—first in simulation and then easily in hardware implementation. They address loading issues with buffer op amps.

In this scenario, the students are "playing the game" from the start. In the past, I have decried engineering silos and engineer comfort zones, both in industry and academia, as the two biggest obstacles to innovation. Add this educational deficiency to that list. Let's get our heads out of the sand! EDN

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An introduction to ACOUSTIC THERMOMETRY

USE AN ULTRASONIC TRANSDUCER TO MEASURE AIR TEMPERATURE IN AN OLIVE JAR.

BY JIM WILLIAMS AND OMAR SANCHEZ-FELIPE • LINEAR TECHNOLOGY

Acoustic thermometry is an arcane, elegant technique that measures temperature using the temperature-dependent transit time of sound in a medium (**references 1** through **4**). The medium can be a solid, a liquid, or a gas. Acoustic thermometers function in environments, including extreme temperatures, destructive physical abuse, and nuclear reactors, that conventional sensors cannot tolerate. Sonic speed in air varies predictably as the square root of temperature. The sonic transit time in a gas-path thermometer is almost entirely insensitive to pressure and humidity. Gas-path acoustic thermometers respond quickly to temperature changes. They have essentially no thermal mass or lag.

AT A GLANCE

- Acoustic thermometers function in environments that conventional sensors cannot tolerate.
- You can measure air temperature by the speed of sound.
- Barometric pressure is not a primary variable.
- The signal path requires careful design.
- Gating can be used to reduce noise and ignore spurious signals.
- A microprocessor calibrates the design to 0.1°F resolution.

IMAGE: THINKSTOCK

You take a measurement across the entire body of an acoustic thermometer. The measurement represents the total path-transit time. Conventional sensors, in contrast, measure at a single point. An acoustic thermometer is thus blind to temperature variations within the measurement path. It infers temperature from the isothermal or the nonisothermal measurement path's delay.

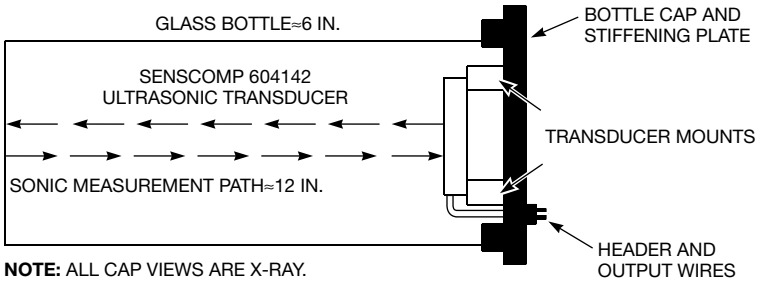

Figure 1 The ultrasonic transducer rigidly mounts within the stiffened cap you affix to a glass bottle.

PRACTICAL CONSIDERATIONS

A practical acoustic-thermometer demonstration begins with selecting a sonic transducer and a dimensionally stable measurement path. A wideband ultrasonic transducer promotes fast, low-jitter, high-fidelity response free of resonance and other parasitic losses. An electrostatic ultrasonic sensor (**Figure 1**) meets these requirements (**Reference 5**). An ultrasonic transducer serves as both transmitter and receiver. The device is rigidly mounted on the metal cap of a glass enclosure. You should stiffen the cap to ensure dimensional stability of the measurement path. This design uses the bottle and cap from Reese (http://reese.elsstore.com) Cannonball olives (**Figure 2**). Barometric pressure is not a major variable in transit time because it does not bow the stiffened cap, averting errors.

You should remove the olives and their residue, and bake out the bottle and cap at 100°C. Pass the transducer leads through the cap using a coaxial header. The glass enclosure has a relatively small thermal-expansion coefficient. This arrangement makes the path distance stable with temperature, pressure, and mechanical changes. The round-trip path length is approximately 12 in. The speed of sound in air is 1.1 feet/msec. Thus, the round-trip time is 900 µsec. The path's temperature-dependent variation is approximately 1 µsec/°F at 75°F. To achieve a 0.1°F resolution requires mechanical and electronic variations of less than 100 nsec, which in turn requires a 0.001-in. dimensional stability referred to the 12-in. path length. When you examine the likely error sources, you will see this stability as a realistic goal.

You bias the transducer, which acts

Figure 2 A plate of copper-clad PCB material stiffens the metal cap of the olive jar. The transducer mounts inside the jar, and an SMA header allows a coaxial cable to connect to the assembly.

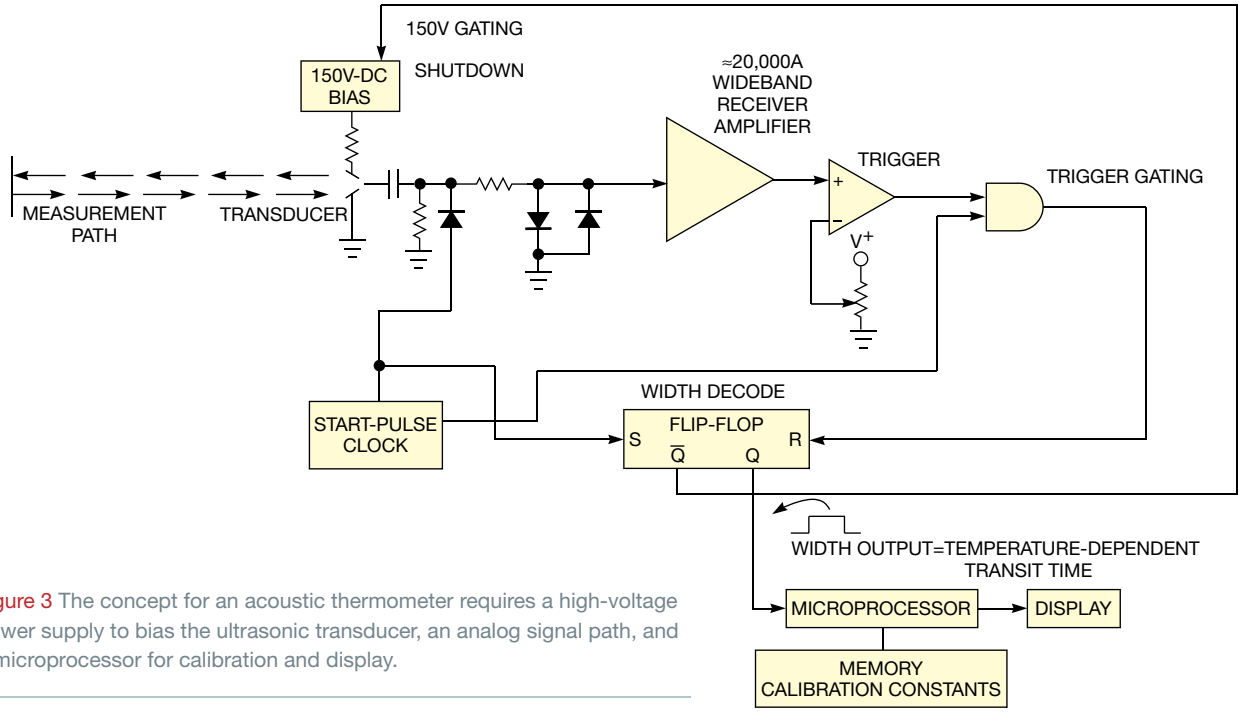

Figure 3 The concept for an acoustic thermometer requires a high-voltage power supply to bias the ultrasonic transducer, an analog signal path, and a microprocessor for calibration and display.

as a capacitor, at 150V dc (**Figure 3**). The start-pulse clock drives the transducer with a short impulse, launching an ultrasonic event into the measurement path. The start-pulse clock simultaneously sets the width-decoding flip-flop high. The sonic impulse bounces off the enclosure's bottom, travels back, and impinges on the transducer, resulting in a minuscule mechanical displacement, which in turn changes the capacitance of the transducer. Based on the **equation** relating charge, Q, to capacitance and voltage, Q=C×V, the capacitance change creates a voltage change at the receiver amplifier's input.

The trigger comparator converts the amplifier's output excursion into a logic-compatible level, resetting the width-decoding flip-flop. The flip-flop's output width represents the measurement path's temperature-dependent

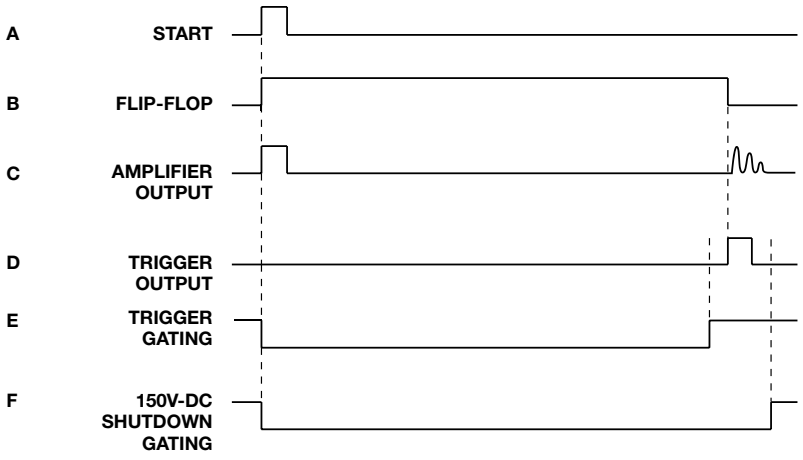

Figure 4 The acoustic thermometer uses a start pulse to drive the transducer (Trace A), setting the flip-flop high (Trace B). The sonic pulse returns (Trace C), activating the trigger output (Trace D) and resetting the flip-flop. You gate the trigger circuit to prevent an erroneous trigger response (Trace E). Another gate turns off the 150V switching converter during the measurement to prevent amplifier corruption (Trace F).

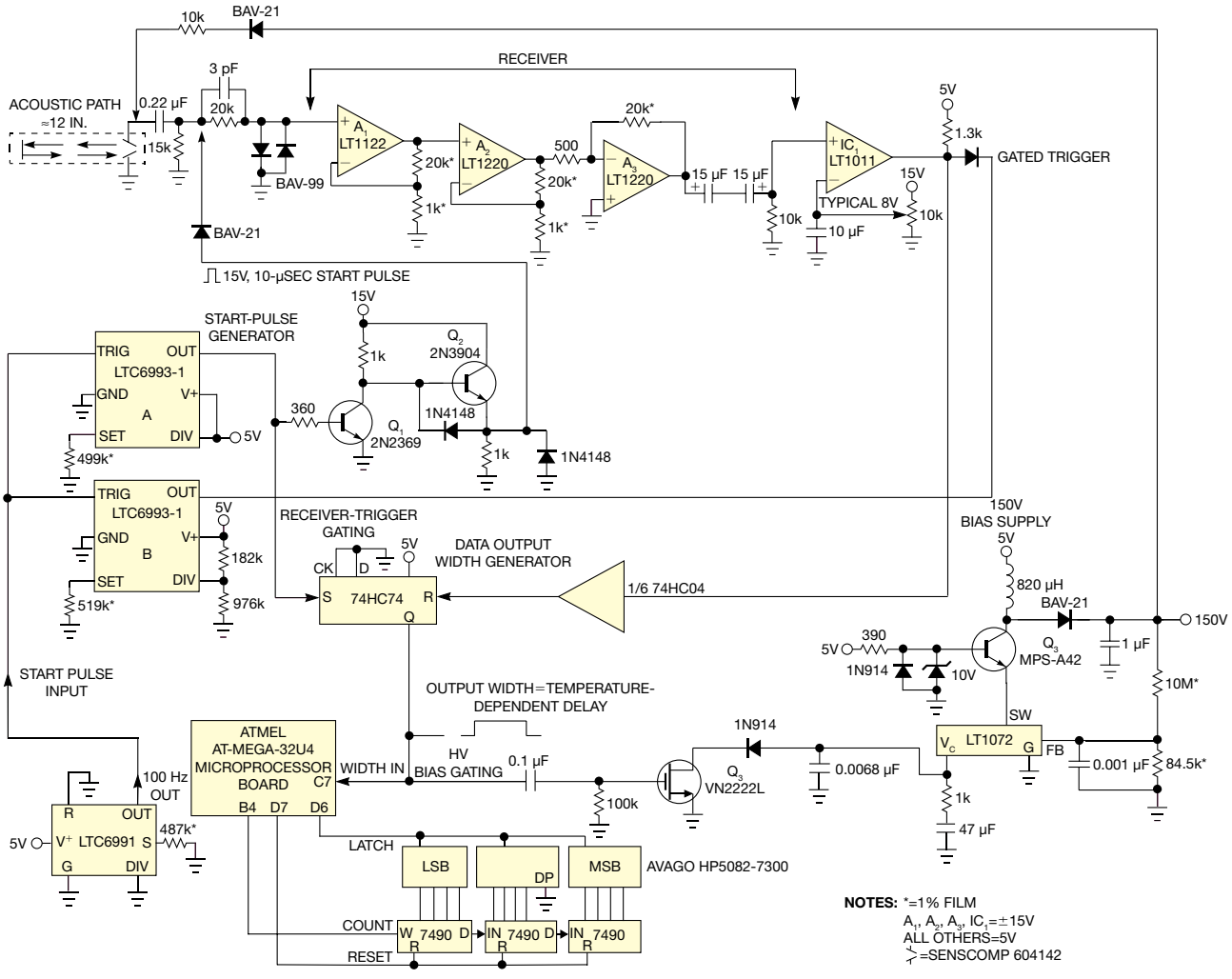

Figure 5 The detailed circuitry closely follows the concepts of those in Figure 3.

sonic transit time. You program the microprocessor with the measurement path's temperature and delay calibration constants (see **sidebar** "Measurement-path calibration"). The microprocessor can then calculate the temperature using the pulse width and supply this information to the display.

You derive a second output from the start-pulse generator, which gates off the trigger's output during most of the measurement cycle, enabling the trigger output only during the time when you expect a return pulse. This method eliminates false triggers by discriminating against unwanted sonic events that originate outside the measurement path. The transducer's return pulse amplitude is less than 2 mV. The high-gain, wideband receiver amplifier is vulnerable to parasitic inputs, so you must shut down the 150V bias supply during the measurement to prevent its switching harmonics from corrupting the amplifier. You derive a second gate from the width-decoding flip-flop. It shuts down the 150V bias supply during the measuring interval.

A measurement cycle begins with a start pulse driving the transducer (Trace A in **Figure 4**), setting the flip-flop (Trace B) high. After the sonic impulse's transit time, the amplifier responds (Trace C), tripping the trigger, which resets the flip-flop (Trace D). The gate signals protect the trigger from unwanted sonic events, start-pulse artifacts, and shut off the high-voltage regulator during measurement (traces E and F).

DETAILED CIRCUITRY

A silicon oscillator furnishes the 100-Hz clock (**Figure 5**). Monostable pulse generator IC_A provides a 10-µsec pulse to a driver you make with Q_1 and Q_2. You capacitively couple the driver output's start pulse into the ultrasonic transducer (Trace A in **Figure 6**). The monostable

MEASUREMENT-PATH CALIBRATION

Theoretically, you can calculate temperature-calibration constants from the measurement-path length. In practice, it is difficult to determine the path length to the required accuracy because of glass-jar, transducer, and mounting dimensional uncertainties. Instead, you must calibrate the device over known temperatures (Figure A). Place the enclosure in a controllable thermal chamber with an accurate thermometer and ensure that the thermometer is isothermal with the enclosure. Next, vary the chamber temperature over 10 evenly spaced points at 60 to 90°F. The enclosure has a 30-minute time constant to settle within 0.25°F. You must allow adequate time for each step to stabilize before taking readings. Note the pulse width at each temperature and record the data. You then load this information into the microprocessor memory.

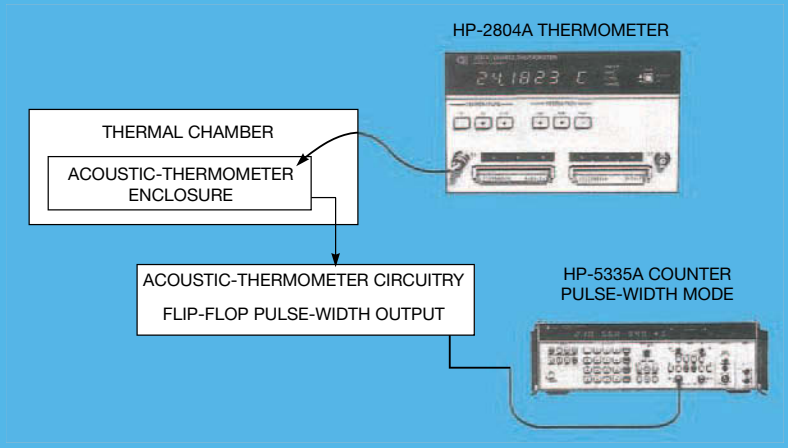

Figure A The calibration arrangement comprises a thermometer, a counter, acoustic-conditioning circuitry, and the glass-jar enclosure inside a thermal chamber.

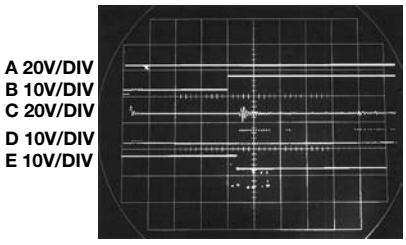

Figure 6 The schematic waveforms include the start pulse (Trace A), the trigger gate (Trace B), amplifier A_2's output (Trace C), the trigger output (Trace D), and the flip-flop's output (Trace E). The second acoustic bounce causes a second set of trigger outputs, which are inconsequential to the circuit's operation (Trace D).

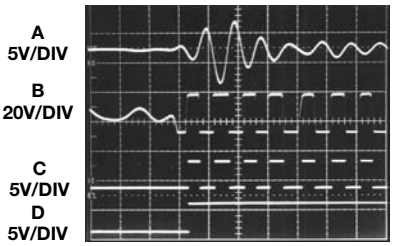

Figure 7 You monitor the amplifier's response at the output of A_2 (Trace A). Amplifier A_3 adds gain, which softly saturates the signal's leading-edge response (Trace B). Comparator IC_1's trigger output creates multiple triggers (Trace C). However, the flip-flop output remains high after the initial trigger, providing an accurate transit time (Trace D).

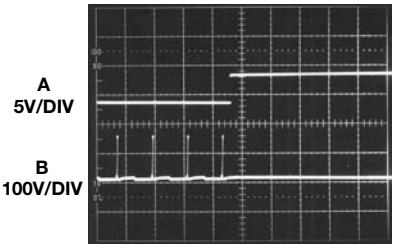

Figure 8 The high-voltage bias-supply-gate signal (Trace A) disables the 150V converter-flyback events (Trace B).

pulse generator simultaneously sets the flip-flop high (Trace E). The high output from the flip-flop shuts down the high-voltage switching regulator during the measurement. You set up the monostable pulse generator, IC_B, to produce a second pulse. This pulse gates off comparator IC_1's output for a time just shorter than the expected sonic return pulse (Trace B).

The sonic pulse travels down the measurement path, bounces, and returns to impinge on the transducer. The switching regulator biases the transducer at 150V dc. It operates as a cascode of the internal switching transistor in the IC and high-voltage transistor Q_3. This high voltage allows the small capacitance change that the diaphragm's motion creates to generate an appreciable voltage change. You send this voltage change to the receiver amplifier. Capacitive coupling isolates the high-voltage dc-transducer bias, and diode clamps prevent destructive overloads. The cascaded receiver amplifier has an overall gain of 17,600. You can monitor the amplifier at the low-impedance output of A_2 (Trace C). A_3, the last stage in the cascade, further amplifies the signal. You send the amplifier output to comparator IC_1, which creates an output trigger (Trace D) that occurs at the first event that exceeds its negative-input threshold. The trigger resets the width-decoding flip-flop. The flip-flop pulse width then represents the temperature-dependent acoustic transit time. You send this pulse to the microprocessor, which determines and displays the temperature (**Reference 6**). See **sidebar** "Software code" in the Web version of this article at www.edn.com/110421df for the complete processor-software code.

You can expand your oscilloscope's signals at the return impulse trip point (**Figure 7**). You monitor the amplifier's response at the output of A_2 (Trace A). Amplifier A_3 adds gain, which softly saturates the signal's leading-edge response (Trace B). Comparator IC_1's trigger output creates multiple triggers (Trace C). However, the flip-flop output remains high after the initial trigger, providing an accurate transit time (Trace D).

Gate the high-voltage supply to prevent switching harmonics from producing spurious amplifier outputs. The start pulse sets the flip-flop output high (Trace A in **Figure 8**), shutting down high-voltage switching at the onset of the measurement period (Trace B). This state persists during the entire transit time and prevents erroneous amplifier-trigger outputs. A return-pulse trigger resets the flip-flop (Trace A in **Figure 9**). You send the flip-flop output to a circuit that gates off the switching regulator by modulating its compensation pin, V_C, delaying the high-voltage turn-on until after the measurement period (Trace B) and ensuring a clean, noise-free trigger signal.

Gating the trigger output prevents interference from outside sources. Gating the 150V converter prevents its harmonics from corrupting the receiver's amplifier. The 150V supply value is a gain term. The higher it is, the more signal it returns. Gating off its regulation during the measurement is a potential concern. Practically, the 1-µF output capacitor decays only 30 mV, or approximately 0.02%, during this time. This small variation is constant and insignificant, and you can ignore it. You derive the trigger trip point and the start pulse from the same 15V supply, enhancing stability because it makes the trigger voltage vary ratiometrically with the received signal's amplitude. The wideband, highly sensitive, and resonance-free transducer descends from 1970s-era Polaroid (www.polaroid.com) SX-70 automatic-focus cameras, promoting repeatable, jitter-free operation. All of these attributes

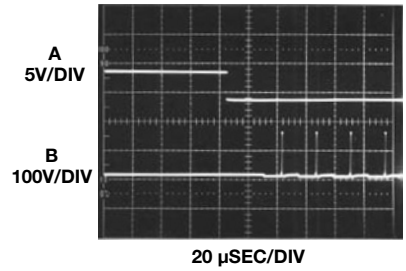

Figure 9 When the high-voltage bias-supply gate falls (Trace A), the supply resumes operation.

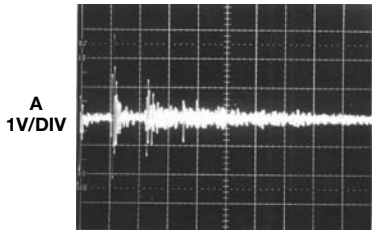

Figure 10 The circuit can detect multiple bounces of the original sonic pulse. By the fourth bounce, sonic dispersions in the jar cause almost total loss of the signal.

directly contribute to the 100-nsec, 0.1°F resolution of the circuit for a 1-msec travel time, representing less than 100-ppm uncertainty. Once you calibrate the circuit, the absolute accuracy at 60 to 90°F is within 1°F.

Further investigations might have you attempt to trigger the receiver after multiple bounces (**Figure 10**). This approach offers the benefit of easing timing tolerances. The return signals decay into noise that acoustic dispersion in the glass enclosure creates. Triggering on a later bounce would relax your timing margins but also gives you an unacceptable SNR (signal-to-noise ratio). Signal-processing techniques could overcome this problem, but the effort would have to justify the increased resolution. EDN

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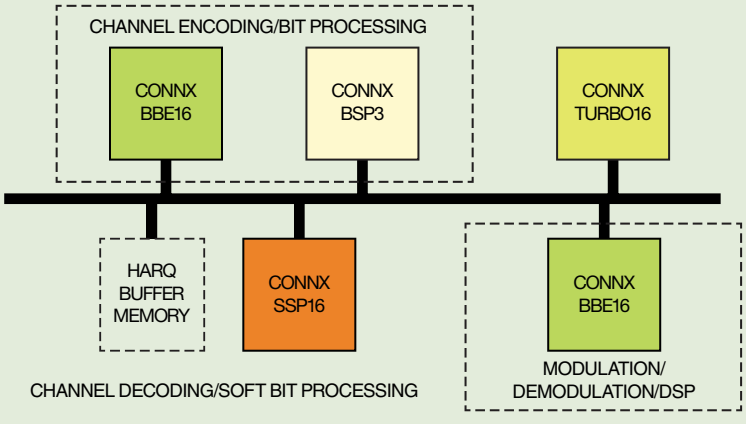
DSPs POWER the RACE to 4G

BY MIKE DEMLER • TECHNICAL EDITOR

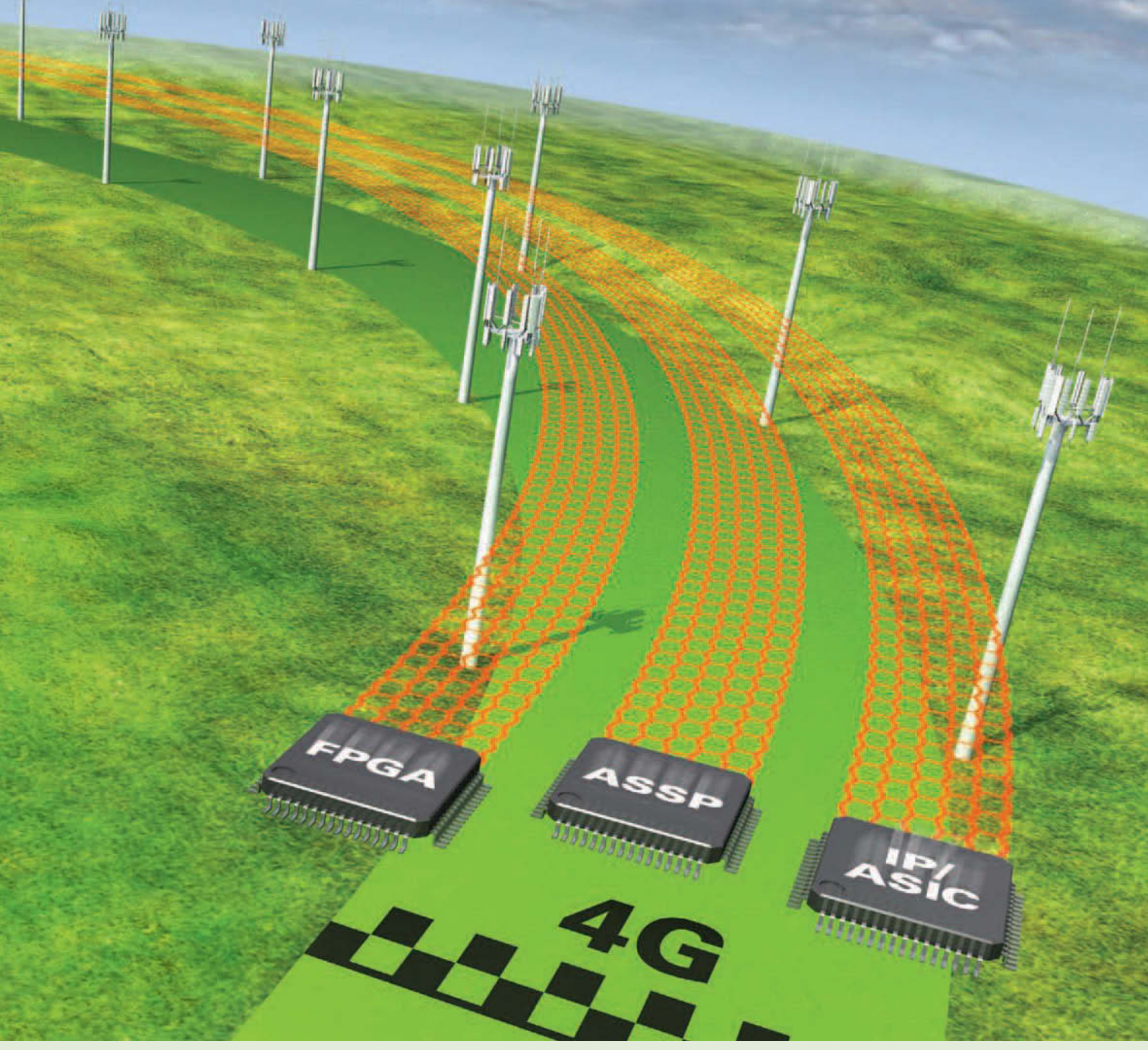
The evolution of wireless mobile broadband technology from 3G (third-generation) to 4G (fourth-generation) networks has given rise to considerable marketing hype. The "official" 4G technologies, which the ITU (International Telecommunication Union) designates, are LTE (long-term-evolution)-Advanced and WirelessMAN (metropolitan-area-network)-Advanced, which is perhaps better known as WiMax (worldwide interoperability for microwave access), or IEEE 802.16m. Nevertheless, these facts haven't stopped a few wireless operators—AT&T and T-Mobile in the United States, for example—from appropriating the designation for their new and improved 3G networks. The companies are boosting their network speed with HSPA+ (evolved high-speed-packet-access) services. The manufacturers generally base these pseudo-4G mutants on software upgrades to 3G base stations, usually with some additional enhancements to the backhaul connection.



BBE: BASEBAND ENGINE
BSP: BROADBAND SIGNAL PROCESSOR
DSP: DIGITAL-SIGNAL PROCESSOR
HARQ: HYBRID AUTOMATIC-REPEAT REQUEST

Figure 1 Tensilica's Atlas LTE reference-architecture platform implements a 3GPP LTE Layer 1 PHY with components of the ConnX DSP family.

Verizon Wireless, backing LTE, and Sprint and Clearwire, backing WiMax, have begun the transition to the all-IP (Internet Protocol) network architectures that are mandatory for a legitimate 4G system, as has TeliaSonera in Europe, albeit with considerably lower data rates than the 1-Gbps download speed that the ITU-endorsed versions specify. Regardless, if you are designing cellular base stations for either system, you know the reality: 4G's higher data rates and lower communications latency place much heavier demands on the DSP (digital-signal-processing) components that execute the underlying communication algorithms. LTE specifies a maximum download data rate of 150 Mbps versus HSPA+'s 42 Mbps, and the maximum upload rate increases from 11 to 75 Mbps in LTE.



Next-generation base stations speed mobile connectivity with SDRs, hard-coded accelerators, and multicore CPUs.

Industry-standards organization 3GPP (Third Generation Partnership Project) denotes the enhanced 4G base stations as eNodeB (Evolved NodeB, **Reference 1**). To deliver the coverage, capacity, and throughput demands of 4G, wireless operators must build heterogeneous networks by linking base stations of various sizes—from small femtocells that support just a few users in a residential or an enterprise setting, to whole-building picocells, to wide-area microcells and macrocells that can simultaneously support hundreds or thousands of users. Operators are also managing the 4G rollout by installing multimode base stations with SDRs (software-defined radios) that simultaneously support both 3 and 4G. The scalability of your base-station-DSP design is critical.

Fortunately, as a designer of an eNodeB system, you have a lot to choose from when it comes to DSP components. If you are developing an LTE SOC (system on chip), several silicon-IP (intellectual-property) vendors can provide most of the building blocks that you need in a customizable form that you can fine-tune for your ASIC. Alternatively, you can find off-the-shelf DSP ASSPs (application-specific standard processors) that support LTE or WiMax process-

ing. At the 2011 MWC (Mobile World Congress) in Barcelona, Spain, several chip companies made competing claims to having developed the first complete LTE base station on a single chip. A third option is also available, with new FPGAs offering much of the customizability of an ASIC with the DSP-hardware performance of an ASSP. It pays to compare before you decide which 4G DSP vehicle is best for your application.

4G DSP BUILDING BLOCKS

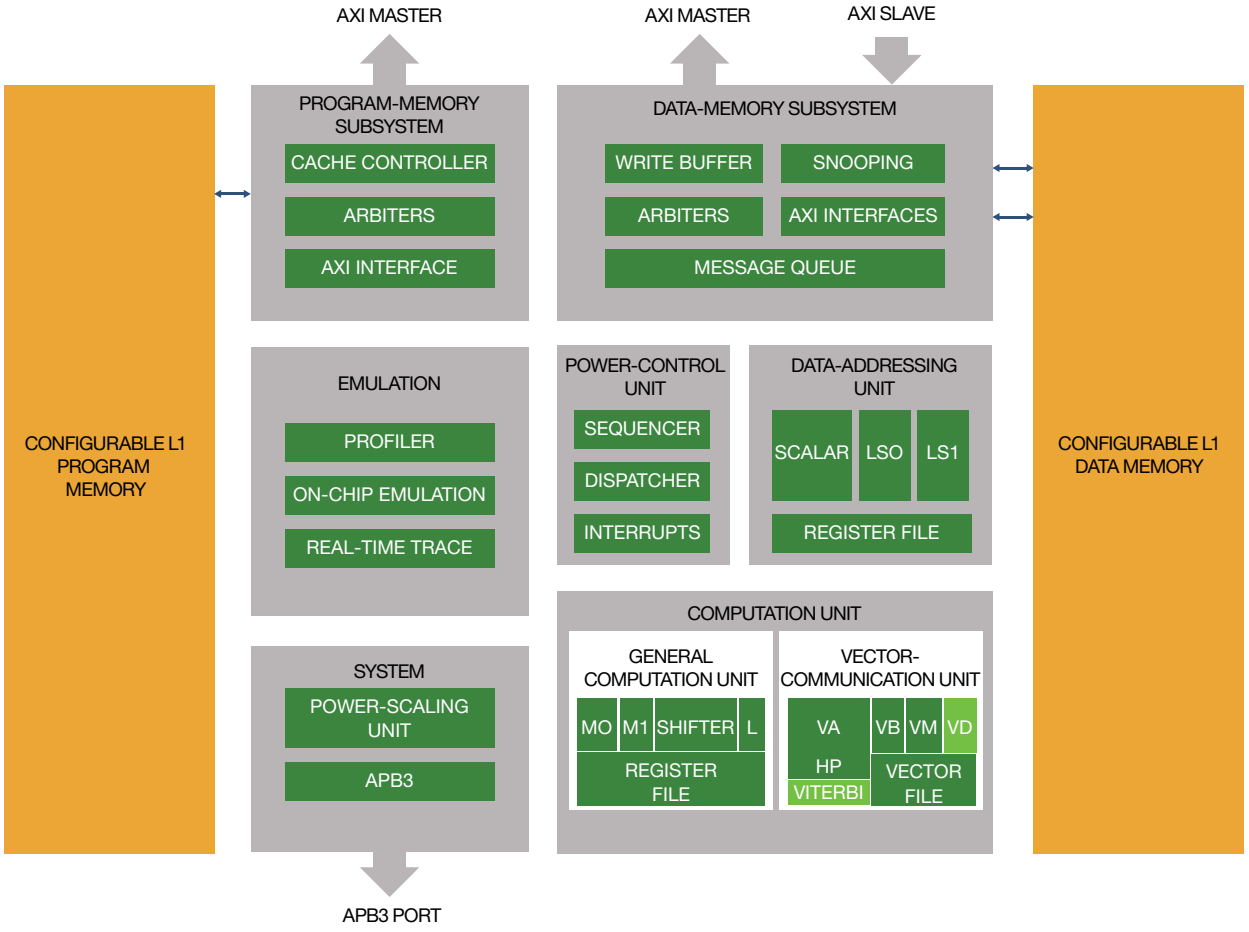
To build a 4G modem, you must start with the PHY (physical) layer, Layer 1 or the radio-interface layer. To exploit the high data rate and spectral efficiency of 4G radio technologies, which are similar for LTE and WiMax, designers apply sophisticated DSP for the OFDMA (orthogonal-frequency-division/multiple-access) modulation with as much as 64-QAM (64-state quadrature-amplitude modulation); the interface to MIMO (multiple-input/multiple-output) antennas with adaptive beam forming; and a host of sophisticated techniques for packet processing, error control, and QOS (quality of service). The 3GPP industry-standard organization is now up to Release 9 of its LTE specification, and more changes should emerge as the organization further develops Release 10 and beyond for LTE-Advanced.

AT A GLANCE

- The growth of 4G (fourth-generation) wireless networks will drive deployment of a heterogeneous mix of base stations.
- Multimode SDRs (software-defined radios) are necessary to overlay emerging 4G networks with legacy 3G (third-generation) infrastructure.
- Designers must combine fixed-function hardware accelerators with multicore DSPs and RISC (reduced-instruction-set-computer) CPUs to achieve required performance.

Tensilica has developed the Atlas LTE reference-architecture platform, which implements a complete 3GPP LTE Layer 1 PHY with components of the ConnX DSP family (**Figure 1**). You can modify the fully programmable Atlas SDR after manufacture of an SOC to accommodate changes in the LTE standard. The ConnX BBE (baseband engine) 16 contains 16 18×18-bit MAC (multiply/accumulate) units that can perform FFTs (fast Fourier transforms) or other digital-filter functions and an eight-way SIMD (single-instruction/multiple-data), three-issue, VLIW (very-long-instruction-word) vector-processing pipeline.

The Atlas often offloads bit-manipulation functions to the ConnX BSP3, which targets 16-, 20-, 32-, and 40-bit vector operations, and performs com-



APB: ADVANCED PERIPHERAL BUS
AXI: ADVANCED EXTENSIBLE INTERFACE
HP: HIGH PRECISION
L1: LEVEL ONE
LS: LOGIC OPERATIONS
M1: MULTIPLY/ACCUMULATE CIRCUIT
MO: MULTIPLY/ACCUMULATE CIRCUIT
VA: VECTOR ARITHMETIC
VB: VECTOR BIT MANIPULATION
VD: VECTOR DATA

Figure 2 The high-performance Ceva XC323 licensable IP core for 4G SDR base-station applications features dual vector-processing engines.

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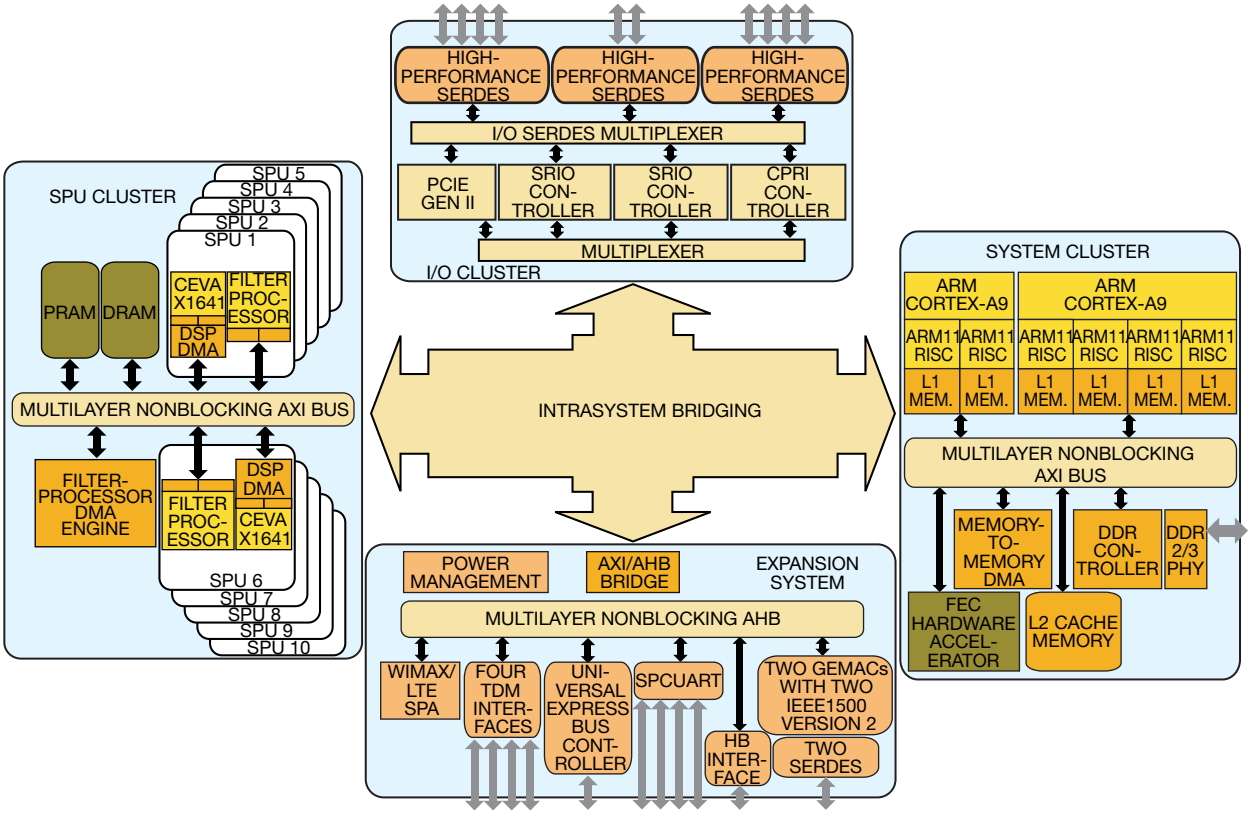
putations on 128-bit-wide vector files that it can load and store as four 32-bit words, eight 16-bit words, or 16 8-bit words. The ConnX Turbo16 LTE turbo performs the LTE-turbo-coding function on data streams operating as fast as 150 Mbps, and it is programmable so that you can modify the software algorithms for various data sources and formats. The 16-way SIMD ConnX SSP16 arithmetic processor processes streams of soft bits to perform functions such as LTE HARQ (hybrid-automatic-repeat-request) error-correction coding. You can add optional specialized functions, such as a Viterbi-accelerator module, to the SSP16.

Tensilica recently extended the BBE family with the ConnX BBE64-128, increasing performance to more than 100 billion MAC operations to meet future requirements for LTE-Advanced (**Reference 2**). The BBE64-128 enables 128 MAC operations per cycle for maximum throughput and minimum energy consumption. Modeless switching to Tensilica's smaller standard 16- and 24-bit instructions enables high code density for nonvector algorithms.

The high-performance Ceva XC323 licensable IP core for 4G SDR base-station applications features dual vector-processing engines (**Figure 2**). Ceva's DSP core integrates an eight-way VLIW SIMD architecture in a 2×256-bit configuration for as many as four parallel operations in each processor, with 32 MAC operations per cycle. The core also has built-in native support for complex arithmetic. The Ceva-XC323 is scalable for base stations from femtocells to macrocells, and the architecture supports 3G standards, such as WCDMA (wideband-code division/multiple access) and HSPA as well as 4G WiMax, LTE, and LTE-Advanced. The XC323 software supports nonvectorized operations, and the instruction sets cover a full range of Layer 1 PHY requirements such as DFT (discrete Fourier transform), FFT, channel estimation, MIMO detectors, an interleaver, a deinterleaver, and optional support for Viterbi decoding. Ceva based the XC323's GCU (general computation unit) on the Ceva-X1641. The device provides four-issue SIMD operation and four 16×16-bit two's-complement MAC units and four 40-bit ALUs (arithmetic-logic units).



AHB: ADVANCED HIGH-PERFORMANCE BUS
AXI: ADVANCED EXTENSIBLE INTERFACE
CPRI: COMMON PUBLIC-RADIO INTERFACE
DDR: DOUBLE DATA RATE
DMA: DIRECT-MEMORY ACCESS
DRAM: DYNAMIC RANDOM-ACCESS MEMORY
DSP: DIGITAL-SIGNAL PROCESSOR
FEC: FORWARD-ERROR CORECTION
GEMAC: GIGABIT-ETHERNET MEDIA-ACCESS CONTROLLER
GPIO: GENERAL-PURPOSE INPUT/OUTPUT
I/O: INPUT/OUTPUT
L1: LEVEL 1
L2: LEVEL 2
LTE: LONG-TERM EVOLUTION
PCIE: PERIPHERAL COMPONENT INTERCONNECT EXPRESS
PHY: PHYSICAL LAYER
PRAM: PHASE-CHANGE RANDOM-ACCESS MEMORY
RISC: REDUCED-INSTRUCTION-SET COMPUTER
SERDES: SERIALIZER/DESERIALIZER
SPA: SECURITY-PROCESSOR ACCELERATOR
SPI: SERIAL-PERIPHERAL INTERFACE
SPU: SIGNAL-PROCESSING UNIT
SRIO: SERIAL RAPIDIO
TDM: TIME-DIVISION MULTIPLEXING
UART: UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

Figure 3 Mindspeed describes the Transcede 4000 as the first commercially available single-chip eNodeB product for LTE small cells.

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By applying the instruction-level parallelism in the XC323, you can parallelize as many as eight control and vector instructions. You can construct a homogeneous multicore system design by connecting multiple instances of the XC323 through the built-in AXI (advanced-extensible-interface) bus. A snooping mechanism in the data-memory subsystem removes handshake overhead by detecting external-device accesses to internal memory buffers. The data-memory subsystem also contains a message queue for synchronization and system control and control for access to external memories to enable data sharing among multiple cores. Designers can take advantage of the multilayer AXI concept to implement programmable arbitration between masters and slaves.

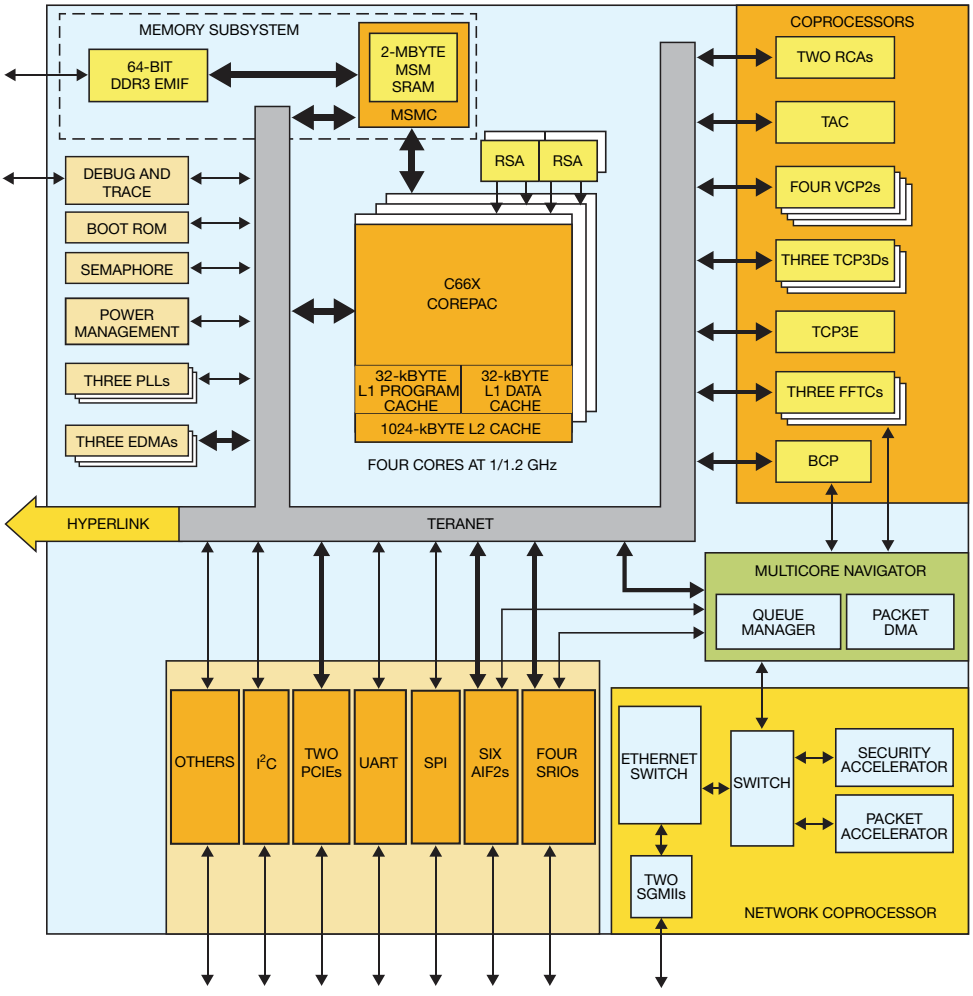
The XC323's PSU (power-scaling unit) has built-in static- and dynamic-power management and supports multiple voltage domains for the various functional units. To conserve energy, you can operate the XC323 core in multiple modes ranging from full operation to memory-retention mode to complete power shutoff. The full-duplex AXI bus also contains low-power features, including the ability to shut down when no data traffic is present.

BASE STATIONS ON CHIPS

Competing claims emerged at the 2011 MWC for the first complete base station-on-chip design. In live demonstrations with partners AirWalk Communications and Lime Microsystems, Mindspeed Technologies showed working production silicon for the Transcede 4000 SOC, which the company initially announced with backing from three presilicon customers in 2010 (**Reference 3**). Mindspeed describes the Transcede 4000, which is a finalist for the 2010 *EDN* Innovation Awards in the ASSP category, as the first commercially available single-chip eNodeB product for LTE small cells (**Figure 3** and **Reference 4**). Mindspeed is manufacturing the 300-Mbps transistor chip in a 40-nm TSMC (Taiwan Semiconductor Manufacturing Co) process.

Alan Taylor, marketing director for wireless-baseband products at Mindspeed, says that a targeted, multicore SOC is the best method of minimizing power and cost and meeting the high-performance DSP requirements of 4G baseband processing. He also notes that scalability is essential as network operators migrate from 3G as 4G standards for LTE continue to evolve. General-purpose DSPs lack the needed precision, Taylor says, and performance requirements drive the need for dedicated fixed-function processors to eliminate the overhead of implementing functions such as FFTs in software. He believes that offloading fixed functions to FPGAs, as has been common in base-station designs, introduces additional power consumption and cost.

The complex, heterogeneous Transcede 4000 SOC integrates 26 programmable processors. The PHY layer includes 10 instances



AIF: ANTENNA INTERFACE
BCP: BIT-RATE COPROCESSOR
DMA: DIRECT-MEMORY ACCESS
EDMA: ENHANCED DIRECT-MEMORY ACCESS
EMIF: EXTERNAL-MEMORY INTERFACE
FFTC; FAST-FOURIER-TRANSFORM COPROCESSOR
I²C: INTER-INTEGRATED CIRCUIT
MSM: MULTICORE SHARED MEMORY
MSMC: MULTICORE SHARED-MEMORY CONTROLLER
PLL: PHASE-LOCK LOOP
ROM: READ-ONLY MEMORY
RSA: RAKE-SEARCH ACCELERATOR
SGMII: SERIAL GIGABIT MEDIA-INDEPENDENT INTERFACE
SPI: SERIAL-PERIPHERAL INTERFACE
SRIO: SERIAL RAPIDIO
TAC: TRANSMIT-ACCELERATOR COPROCESSOR
TCP: TURBO-DECODER COPROCESSOR
UART; UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER
VCP: VITERBI-DECODER COPROCESSOR

Figure 4 TI's TCI6618 targets use in the high-end-base-station market for macrocell or compact-macrocell applications.

of Ceva's 1641 DSP-IP core and 10 Mindspeed DSP accelerators in the SPU (signal-processing-unit) cluster. The microcoded processors accelerate fixed functions, and the Ceva cores handle general-purpose programmable-DSP functions. Mindspeed can remap the microcoded accelerators to suit various applications if necessary.

"It's not just a matter of throwing some network processors and some general-purpose DSPs onto a chip," says Taylor. You must know the architecture so that you know the required speed across the whole system, and you must ensure that you have the right amount of memory and use a nonblocking architecture, he adds. The Transcede 4000 intelligently allocates memory with smart DMA (direct-memory-access) engines, which perform dynamic allocations between the PHY and Layer 2 switch-level or MAC (media-access-controller) functions.

The system cluster performs control functions and data-packet processing, using a combination of dual- and quad-core ARM Cortex-A9 processors in an SMP (symmetric-multiprocessing) configuration. The control plane requires RISC (reduced-instruction-set-computer) processors because they enable the completion of instructions in one cycle. A task dispatcher that runs on one of the ARM cores performs dynamic load balancing. The dispatcher assigns a list of tasks to the next available DSP to run in the local DSP memory. This approach alleviates the need for complex software design and makes the architecture modular and extensible. You can replace Mindspeed-defined tasks with your own differentiated algorithms. Because the dispatcher recognizes the hardware architecture, your software scales with the number of processors in a system. The ARM RISC processors perform packet-processing functions, such as branch prediction, Taylor says, and these functions don't fit well with DSP architectures that must process tight algorithm loops and deep vector processing.

INTEGRATED ARCHITECTURE

Freescale Semiconductor's new QorIQ Qonverge architecture provides an integration of communications-processing, DSP, and wireless-acceleration technologies in various SOC configurations that can work in 3 and 4G femtocell, picocell, metrocell, and macrocell base

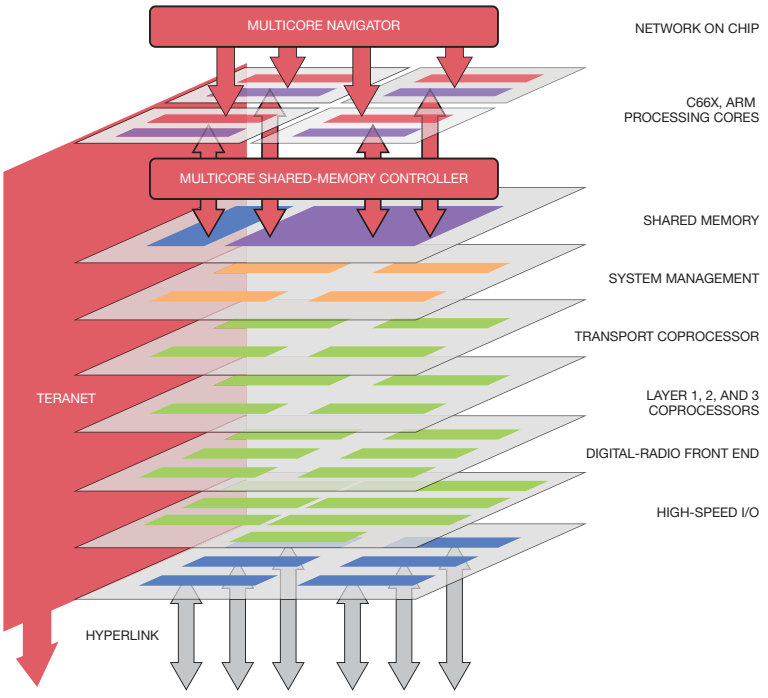


Figure 5 TI's KeyStone architecture, a common platform for scaling C66x designs, includes the TeraNet switch fabric, which provides 2 Tbits of bandwidth for data transfer within the SOC.

stations. Qonverge combines the Power Optimization with Enhanced RISC Architecture CPU core of the original QorIQ communication processor, which Freescale (formerly, Motorola) developed through collaboration with IBM, with a StarCore DSP and MAPLE (multiaccelerator-platform-engine) multimode baseband accelerator. According to Preet Virk, leader of the global-networking-segment marketing division at Freescale, the company has been shipping multicore silicon for the QorIQ since 2009.

At the 2011 MWC, Freescale preannounced the PSC9130/PSC9131, which you will be able to use in femtocell applications to support eight to 16 users. The PSC9130/31 will support LTE in FDD (frequency-division-duplexing) or TDD (time-division-duplexing) configurations at downloading and uploading speeds as high as 100 and 50 Mbps, respectively, as well as 3G CDMA (code-division/multiple-access) and EVDO (evolution-data-optimized) applications. The devices support simultaneous 3 and 4G connections. The MAPLE baseband accelerator provides a turbo/Viterbi decoder and an FFT accelerator.

Freescale also announced the PSC9132, a configuration of the QorIQ Qonverge for picocell and enterprise-femtocell applications. The PSC9132 incorporates two e500 Power Architecture cores and two StarCore SC3850 DSPs, and it extends performance to the full LTE maximum download and uploading speeds of 150 and 75 Mbps, respectively. You can also use the PSC9132 for HSPA+ or in a WiMax 802.16e application to deliver as much as 50- and 13-Mbps downloading and uploading speeds, respectively, for as many as 64 users. The device also includes a CPRI (Common Public Radio Interface) and a MIMO accelerator.

The company is planning to make the PSC9130/31 and PSC9132 available in the second half of this year. Freescale will manufacture the picocell and femtocell products in a 45-nm process. To extend the family for metrocell and macrocell applications, Freescale plans to use a 28-nm process and to have chips available in the early part of 2012. The company did not disclose details of the architecture or the number of embedded cores that future 28-nm designs will integrate. The targeted specifications for the metrocell and macrocell devices support hundreds of users in a single sector of an LTE-Advanced base station or multiple sectors of LTE with 20-MHz channels and as many as eight receiving and transmitting antennas per sector.

TI ADDS ACCELERATORS

At the 2011 MWC, Texas Instruments announced that its new TCI6618 wireless-base-station SOC doubles the performance of the TCI6616, which the company released just six months earlier. According to Kathy Brown, TI's wireless-base-station-product manager, the TCI6618 targets use in the high-end-base-station market for macrocell or compact-macrocell applications (**Figure 4**). The TCI6618 integrates four 1.2-GHz C66x DSP cores that support both fixed- and floating-point arithmetic operations, which is unique to TI's base-station devices, according to Brown. Floating-point operation is especially useful for increasing precision of matrix inversions, she says, resulting in higher spectral efficiency. The TCI6618 is available for sampling, and the company plans volume production for this year. TI will also later announce a device targeting small femtocells and picocells.

According to Ramesh Kumar, TI's worldwide business manager for multicore and media-infrastructure DSPs, customers are increasingly adopting the C66x processor's double-precision floating-point capability for higher dynamic range in a range of DSP applications. You can switch from fixed to floating point on a cycle-by-cycle basis, depending on your algorithm's needs. Kumar points out that this flexibility is not a "natural" function of FPGAs (**Reference 5**).

The TCI6618 has 15 coprocessing accelerators to complement the four DSP cores, performing 95% of the LTE Layer 1 processing. Three TCPD3s (turbo decoder coprocessors) perform turbo decoding, and a TCP3e performs encoding. The product also has four VCP2s (Viterbi-decoder coprocessors) and three FFTCs (fast-Fourier-transform coprocessors). The TCI6618's BRC (bit-rate coprocessor) performs uplink and downlink bit processing for WCDMA/HSPA+, TDSCDMA (time-division-synchronous-code division/multiple access), LTE, and WiMax. It also supports GSM (global-system-for-mobile) communications and CDMA. For LTE, the device supports a data rate as high as 914 Mbps.

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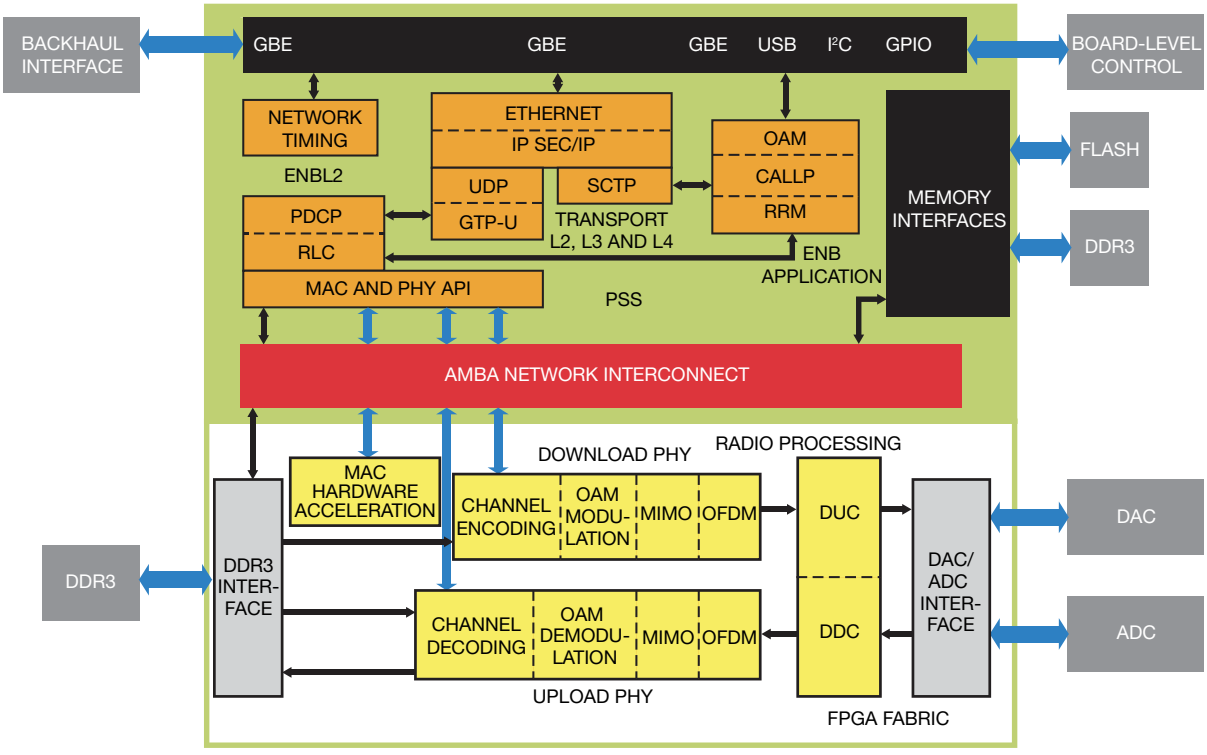

ADC: ANALOG-TO-DIGITAL CONVERTER
AMBA: ADVANCED MICROCONTROLLER-BUS ARCHITECTURE
API: APPLICATION-PROGRAMMING INTERFACE
DAC: DIGITAL-TO-ANALOG CONVERTER
DDC: DIGITAL DOWNCONVERSION
DDR: DOUBLE DATA RATE
DUC: DIGITAL UPCONVERSION
ENBL: ENODEB
FPGA: FIELD-PROGRAMMABLE GATE ARRAY
GBE: GIGABIT ETHERNET
GPIO: GENERAL-PURPOSE INPUT/OUTPUT
GTPU: GENERAL PACKET RADIO SERVICE TUNNELING PROTOCOL-USER PLANE
I²C: INTER-INTEGRATED CIRCUIT
IP: INTERNET PROTOCOL
IPSEC: INTERNET PROTOCOL SECURITY
L1: LEVEL ONE
L2: LEVEL TWO
L3: LEVEL THREE
L4: LEVEL FOUR
MAC: MEDIA-ACCESS CONTROLL
MIMO: MULTIPLE INPUT/MULTIPLE OUTPUT
OAM: OPERATIONS/ADMINISTRATION/MANAGEMENT
OFDM: ORTHOGONAL FREQUENCY-DIVISION MULTIPLEXING
PDCP: PACKET DATA CONVERGENCE PROTOCOL
PHY: PHYSICAL LAYER
PSS: PRIMARY SYNCHRONIZATION SIGNAL
RLC: RADIO-LINK CONTROL
RRM: RADIO-RESOURCE MANAGEMENT
SCTP: STREAM CONTROL TRANSMISSION PROTOCOL
UDP: USER DATAGRAM PROTOCOL
USB: UNIVERSAL SERIAL BUS

Figure 6 Xilinx's Zynq 7000 family of EPP devices allows you to combine the baseband processing and radio interface into one chip for an enterprise femtocell.

A network coprocessor enables communications between the TCI6618 and the network, with a packet accelerator and a security accelerator for autonomous packet-to-packet processing. The network coprocessor handles acceleration for Layer 2 and transport processing. According to TI, the network coprocessor, together with the DSP cores and other acceleration for layers 1 and 2 processing, eliminates the need for a RISC processor.

The TCI6618's multicore navigator decreases programming effort by allowing you to create an abstraction of tasks with priorities that the packet-based manager in the multicore navigator then dispatches to the DSP cores as they become available. This approach is similar in concept to the task dispatcher that runs on one of the ARM cores in Mindspeed's SOC.

TI's KeyStone architecture, a common platform for scaling C66x designs, includes the TeraNet switch fabric, which provides 2 Tbits of bandwidth for data transfer within the SOC (**Figure 5**). The MSMC (multicore-shared-memory controller) enables the cores to directly access shared memory without using any of TeraNet's bandwidth. Peripherals in the TCI6618 include a six-lane AIF2 SERDES (serializer/deserializer)-based antenna interface that operates as fast as 6.144 Gbps and that complies with the OBSAI (Open Base Station Architecture Initiative) RP3 (Reference Point 3) and CPRI Standards. Four Lanes of SRIO (Serial RapidIO) 2.1 and two lanes of PCIe (Peripheral Component Interconnect Express) Generation 2 I/Os support operation as fast as 5 Gbps. A 64-bit DDR3 interface allows you to connect to external memory at speeds as high as 1333 MHz.

The KeyStone architecture indicates the possibility of using an ARM core as the CPU, along with the C66x DSP core. Texas Instruments has designed the switch-fabric infrastructure and shared-memory architecture to accommodate ARM cores and DSP cores in future

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devices but will not announce the first device with ARM cores until mid-2011.

FPGAs EMBED ARM CORES

According to Mark Quartermain, senior manager for the communications business unit at Xilinx, the traditional role of FPGAs in baseband processing is to provide specialized coprocessing accelerators for functions that the DSP does not perform well, such as the turbo decoder, and in connectivity, such as CPRI. He points out that this support is insufficient for 4G, however, for which a single device must provide all the processing to meet data-rate and latency requirements, and instead proposes a linear processing flow with one dedicated FPGA per sector. By replacing the older Virtex-6 FPGAs with the new Kintex-7, you can achieve a 50% reduction in power and cost, says Quartermain.

Xilinx offers a TDP (targeted design platform) for a complete LTE-baseband channel card. You can use the uplink and downlink reference designs, which Xilinx built from a library of optimized prebuilt and prevalidated LogicCore components. The LTE library components include a 3GP P channel decoder and estimator, an LTE FFT, an LTE MIMO, and turbo encoder/decoders. For the radio-interface layer, Xilinx offers the multimode-radio TDP, which you can apply to LTE, TDSCDMA, WiMax, WCDMA, CDMA2000, or GSM applications. LogicCore functions include a crest-factor-reduction block, a digital predistortion filter, digital upconversion and downconversion converters, and CPRI- and SRIO-interface blocks.

With the introduction of the Zynq 7000 family of EPP (extensible-processing-platform) devices, the company allows you to combine the baseband processing and the radio interface into one chip for an enterprise femtocell (**Reference 6** and **Figure 6**). You use the FPGA fabric to implement the uploading- and downloading-channel functions and Layer 1 PHY, and you use the Zynq 7000's embedded dual 800-MHz ARM Cortex-A9 MPCore to execute Layer 2 and higher-layer transport functions. Xilinx based the current LTE TDP reference design on the 32-bit Microblaze RISC-Harvard-architecture soft-processor core. The Zynq 7000 allows you to offload some of the functions of the higher-layer processor to the FPGA fabric, thus accelerating the MAC hardware. EDN

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LED BULBS REVEAL DIFFERENT DESIGN APPROACHES

BY MARGERY CONNER • TECHNICAL EDITOR

A peek into the Philips LED bulb's electronics and the 6W, dimmable Pharox 300 contrasts two approaches in how a bulb handles the protection of the LED-power-control electronics.

A recent article examined light patterns from common lighting bulbs and took apart a Philips (www.philips.com) LED bulb to understand how its use of a secondary phosphor affects its light pattern (**Reference 1**). This article continues that discussion of the Philips 12.5W LED bulb, which relies on a secondary phosphor to spread its light in an almost-360° pattern (**Figure 1**). **Figure 2** shows the top view of the bulb looking down into the wiring and connectors that take the power to the three LED boards.

This bulb uses connectors rather than relying on low-cost labor for hand-soldering, which manufacturers of CFLs (compact fluorescent lamps) use. For example, **Figure 3** shows a view of a PCB (printed-circuit board) from a hand-soldered CFL. The big blobs of solder inspire little confidence in manufacturing quality and probably have played a role in shorter-than-expected lifetimes for some CFLs. Philips' decision to rely on connectors makes for

Figure 1 This 12.5W LED bulb (top left) from Philips produces 800 lumens at a color temperature of 2700K and is warranted for 25,000 hours.

Figure 2 The Philips bulb (top right) uses connectors rather than hand-soldering to bring the wiring around from the back of the board.

a more repeatable, reliable assembly process and should pay off in long-term bulb reliability.

My praise for the use of high-quality connectors resulted in some virtually raised eyebrows in the online comments when I posted these photos online. For example, one reader asked how a connector can be more reliable than a solder joint (**Reference 2**). Because these solder joints are on the top side of the board, they are necessarily hand-soldered, and it's difficult, though not impossible, to achieve a repeatable, high-quality hand-soldered joint in a cramped space in a high-volume manufacturing line. Connectors, on the other hand, are simple to use and consistent in their performance.

Figure 4 shows the LED PCB and connector, as well as the thermal-interface material that helps pull the heat away from the LEDs into the relatively massive heat sink. Popping off the bulb's power socket exposes the power-management circuitry (**Figure 5**) encapsulated in a rubbery potting compound (**Figure 6**). I couldn't get a good photo of the dimming LED-driver IC, but the lettering looked something like CY8OLED, which I believe is a 12W Cypress CY8CLED dimmable LED driver (**Figure 7** and **Reference 3**). When I connected it to a TRIAC (triode-alternating-current) dimmer, the bulb dimmed beautifully from almost 0 to the full 100%.

IT'S DIFFICULT TO ACHIEVE A REPEATABLE, HIGH-QUALITY HAND-SOLDERED JOINT IN A CRAMPED SPACE IN A HIGH-VOLTAGE MANUFACTURING LINE.

My deconstruction of LED bulbs has in the past been utilitarian, relying heavily on hammers, wrenches, and safety glasses (**Figure 8**). Shortly after I performed the Philips bulb tear-down, Peter Di Maso, marketing manager for lighting-power products at Texas Instruments (www.ti.com), told me that he'd had good luck with baking bulbs in the oven

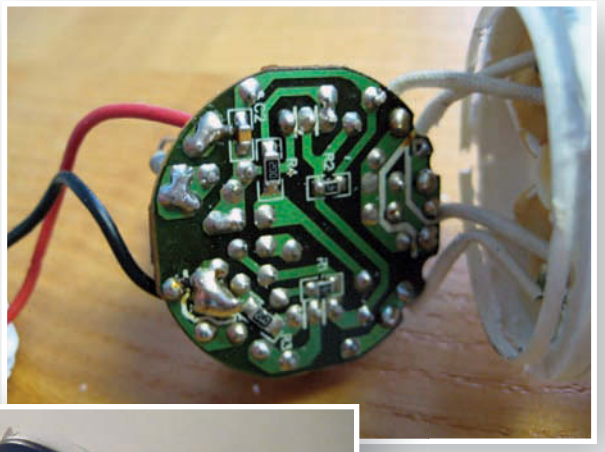

Figure 3 The low-quality hand-soldering on this CFL PCB can shorten the CFL's lifetime.

Figure 4 The LEDs mount vertically on the bulb's heat sink.

Figure 5 The power-management PCB fits into the base of the bulb.

Figure 6 A rubbery potting compound encapsulates the power-management circuitry.

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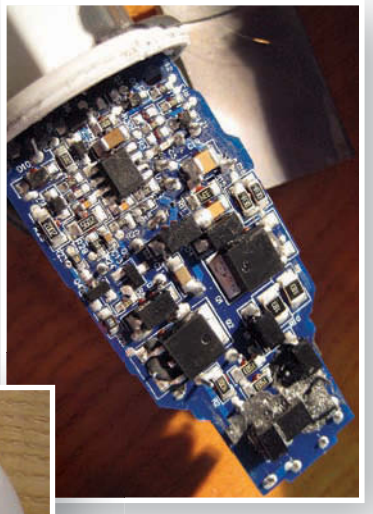

Figure 7 The eight-pin IC (right) looks like a 12W Cypress CY8CLED dimmable LED driver.

Figure 8 Baking a bulb in the oven allows you to pull off the top of a snow-cone bulb, preventing the need for drastic measures such as smashing it (below).

Figure 9 The Pharox 300 bulb (right) has a greater-than-180° light pattern.

at 200°F for 30 minutes before pulling them apart. I tried this approach on my next tear-down. This time, the victim was a Lemnis (www.lemnislighting.com) Pharox 300, a 6W, dimmable LED bulb capable of 360 lumens at 2900K.

Before popping the snow-cone-type bulb into the oven, I turned it on to see its light pattern (**Figure 9**), which turned out to be fuller than the usual 180° you see with a snow-cone-type design. How does the manufacturer achieve that trick? The bulb emitted a noticeable hum, however; I could hear it from 10 feet away.

I had to leave the bulb in the oven for an hour. Wearing leather gloves, I twisted the bulb quite a bit before pulling the white top straight out to reveal an array of six LEDs: Two red LEDs flank four white LEDs, visible in their off-state as yellow (**Figure 10**). This instance marks the first time I've seen "color-tuning" red LEDs in a relatively inexpensive replacement-type LED bulb.

Why would you want to add red to a white light? In general, we associate warmer-colored lights with incandescent lights because most interior color schemes target use with incandescents. However, LEDs are generally more expensive and less efficacious at higher color temperatures. Adding a couple of red LEDs to warm up the white light can make for a more attractive light. George Kelly, an Avnet (www.avnet.com) "illumineer" who spoke at a panel on LED lighting at last month's APEC (Applied Power Electronics Conference, www.apec-conf.org), believes that our preference for warm colors dates back to prehistoric times when firelight was the only option for light at night. Blue light is more prevalent during the day when the sun is high, whereas redder, warmer light is a signal that the day is winding down and it's time to relax.

At this point in the tear-down, the socket was still on the bulb, and I was able to fire up the bulb to see how the red LEDs behaved: They were on whenever the white LEDs were on, dimming and growing brighter in the same way that the white devices were. This scenario contrasts with what I observed in the tear-down of the Cree (www.creelighting.com) TrueWhite LED

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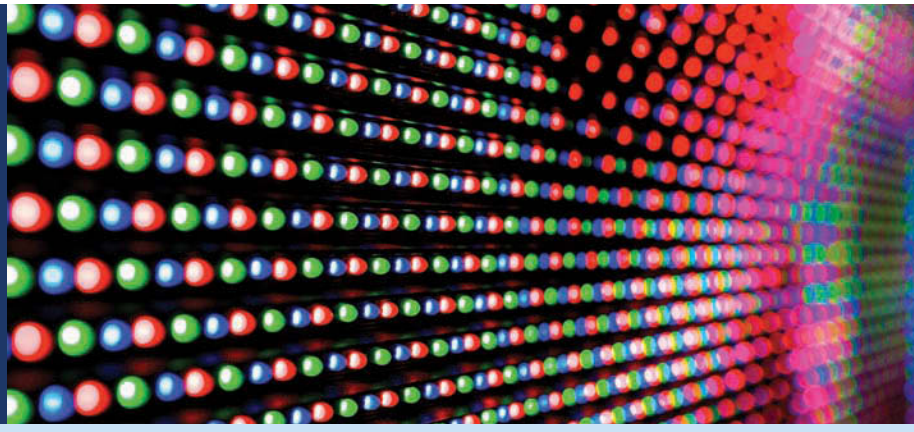

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TECHNICAL TRACKS:

- Power management
- Thermal management
- Optics and light measurement
- Beyond the light: Networking and Solar Power

HIGHLIGHTS:

- Plenary LED manufacturers' panel, featuring representatives from Cree, Lumileds, and Osram, will focus on the relationship between LED drive current and lifetime.
- Lightening talks, and ample networking opportunites.

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Figure 10 Wearing leather gloves, I had to twist the bulb a lot before pulling it straight out to reveal an array of six LEDs.

module, which also uses red LEDs inside the white-LED module (**Reference 4**). However, those red LEDs come on only at full-on power to the module because white LEDs generally shift away from the warmer colors at higher drive currents. The Pharox uses always-on red LEDs to achieve a warmer white but without the added intelligence—and circuitry—of the TrueWhite approach.

Once I got the bulb cover off, I could easily see how the Pharox achieves a larger light pattern than most snow-cone designs (**Figure 11**). The LED's array is slightly elevated. As a result, it projects down more than it would if aligned with the edge of the LED's heat-sink base. The elevation is slight, but the bulb cover, acting as a diffuser, adds a slight reflection, so the light pattern is deeper than that of other snow-cone designs.

Continuing to dismantle the bulb, I removed the base, exposing the power-control electronics (**Figure 12**). This experience marks the first time that I've seen an LED bulb that did not encase its electronic components in a rubbery potting compound, and this lack of compound may be the reason for the audible hum: The potting compound would have either prevented the vibration or muffled the noise from a discrete component. This problem may well have been an isolated one, however.EDN

Figure 11 The LED's array (below) is slightly elevated. As a result, it projects down more than it would if you aligned it with the edge of the LED's heat-sink base.

Figure 12 The power-control electronics (left) are not encapsulated, perhaps contributing to an audible hum from the bulb.

REFERENCES

1 Conner, Margery, "Remote phosphor expands reach of LED light," *EDN*, March 17, 2011, pg 26, http://bit.ly/i0yLXz.
2 Conner, Margery, "Remote phosphors: Philips LED bulb tear-down, part 2," *EDN*, Feb 15, 2011, http://bit.ly/hCo8ft.
3 "CY8CLEDAC02 A55 Highline 12 W Dimmable LED Driver Reference Design Guide," Cypress Semiconductor, http://bit.ly/dM5r4f.
4 Conner, Margery, "Cree's LMR4 LED light module: What's inside and how TrueWhite works," *EDN*, Sept 14, 2010, http://bit.ly/hmlMcT.

EDITED BY MARTIN ROWE
AND FRAN GRANVILLE

designideas

READERS SOLVE DESIGN PROBLEMS

Increase efficiency in embedded digital-I/O lines

Vasile Surducan and Emanoil Surducan, National Institute for R&D of Isotopic and Molecular Technologies, Cluj-Napoca, Romania

Digital-I/O-multiplexing techniques, such as "Charlieplexing" or "Gugaplexing," let an eight-digit, seven-segment LED display connect to nine I/O pins of a microcontroller (**references 1** and **2**). These methods use lower-duty-cycle timing, which requires a driver between the microcontroller's I/O lines and the display to achieve good visibility. The circuit in **Figure 1** uses an 8+N/2 I/O bus for interfacing an N-digit display and as many as eight buttons on the same bus. This method needs no driver. You can apply it to any programmable device with LED-driving capabilities, such as small PIC (www.microchip.com) or Atmel (www.atmel.com) microcontrollers.

In **Figure 1**, R_8 is a segment current-limiting network resistor for the IC_1 common-anode LED display and the IC_2 common-cathode LED display. Any combination of standard and superbright displays for this IC_1/IC_2 pair is acceptable with proper duty-cycle timing adjustment in firmware. The R_7 network and D_1 to D_8 switching diodes act as antighosting devices. "Ghosting," or faint illumination, is the partial illumination of the segments, which should be in an off state, as a result of switching glitches or unsuitable voltage levels on the driving pins when those pins are in a high-impedance

DIs Inside

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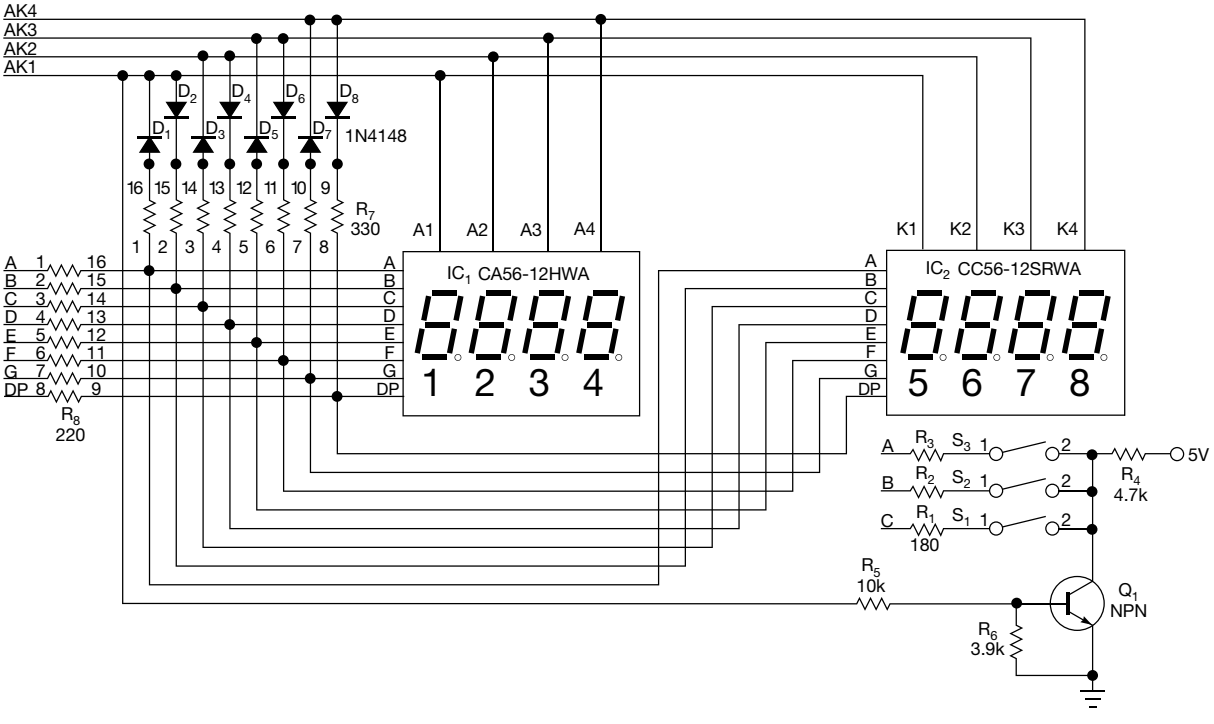
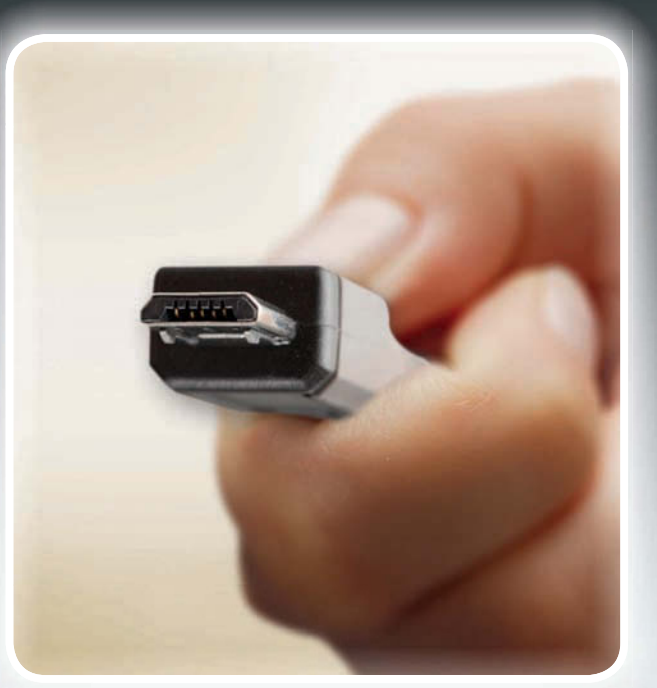


Figure 1 Common-anode and common-cathode LED displays and buttons can connect to the same bus.

Get an Edge: Universal USB Charging

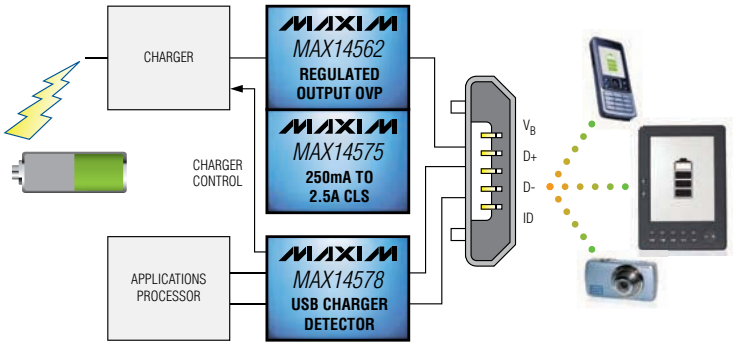
Mess vs. Less



As consumers buy more portable devices, they become overwhelmed with managing power adapters that have a variety of connectors. Solving this issue, the micro USB interface has become the standard for battery charging and data transfer. Maxim's charger detection, overvoltage protection, and current-limit switching ease design-in of micro USB ports to simplify the user experience.

USB Power Adapter Detection

- Enables USB charging (USB Battery Charging Specification, Revision 1.1) from various adapters
- Provides USB dead battery charging support without complex software modification
- High-current switch provides power to enable a wide variety of accessories



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state. Ghosting results from using all the microcontroller's I/O: output-high, output-low, and high-impedance logic levels, switching between them in an infinite-loop sequence (**Table 1**).

The following **equation** calculates the value of R_7: $R_7=(V_{SAFE}–0.6V)/10I_{GHOST}$, where 0.6V is the voltage drop of diodes D_1 through D_8 at 25°C, I_{GHOST} is the threshold value of the static-leakage current for which the ghosting effect is visible but minimal, and V_{SAFE} is the voltage potential value that may appear on any segment when the segment is not illuminated.

You can experimentally find I_{GHOST} at an ambient-light level of less than 10 lux by injecting a small current into a separately powered digit segment and observing the current value and segment voltage drop at the moment when the segment begins to light up. For a superbright display, I_{GHOST} should be approximately 70 µA. The I_{GHOST} current creates an unwanted voltage drop on the segment LED, V_{GHOST}: $V_{GHOST}=1.54V$ and $V_{SAFE}\leq kV_{GHOST}$, where k, a factor of confidence, ranges from 0.5 to 0.7, compensating the V_{GHOST} dispersion of displays. In this example, V_{SAFE} is 0.7V for a superbright LED display and 1V for a standard display. If you combine normal and superbright display types, choose the smallest V_{SAFE} for the computed value of R_7.

Reading electrode buttons is an asynchronous procedure, unlike digital multiplexing; thus, any combination of button presses must not turn on any segment of IC_1's or IC_2's digit group. R_1, R_2, and R_3 limit the current through IC_1 segments below I_{GHOST} when Q_1 is on and AK1 is at an output-high level. R_4, R_5, and R_6 polarize Q_1; R_6 keeps Q_1 off even when AK1 is in a high-impedance state; and R_4 limits the Q_1 collector current. Note that the weak pullup of the A, B, and C microcontroller inputs is on during the button-reading sequence. You can download the firmware source for the PIC16F886 driving the display in **Figure 1** from http://bit.ly/e1cwCu. Adding R_7 and D_1 through D_8 eliminates ghosting (**Figure 2**). EDN

Figure 2 Without R_7, ghosting is visible (left). With R_7, the display is clean (right), even when you push buttons S_1 through S_3.

REFERENCES

1 Sangalli, Luke, "Charlieplexing at high duty cycle," *EDN*, June 25, 2009, pg 44, http://bit.ly/ehxi3w.

2 Gupta, Saurabh, and Dhananjay V Gadre, "Multiplexing technique yields a reduced-pin-count LED display," *EDN*, Oct 16, 2008, pg 58, http://bit.ly/fJhrE8.

TABLE 1 SWITCHING SEQUENCE FOR LED DISPLAYS

Sequence	Display on digit	Read buttons	Common electrode buttons				Segments bus
			AK1	AK2	AK3	AK4	A, B, … D_P
1	IC_1-1	X	High impedance	High impedance	High impedance	High impedance	Output low=data
2	IC_1-2	X	High impedance	High	High impedance	High impedance	Output low=data
3	IC_1-3	X	High impedance	High impedance	High	High impedance	Output low=data
4	IC_1-4	X	High impedance	High impedance	High impedance	High	Output low=data
5	X	Yes	High	X	X	X	Input
6	IC_2-5	X	Low	High impedance	High impedance	High impedance	Output high=! data
7	IC_2-6	X	High impedance	Low	High impedance	High impedance	Output high=! data
8	IC_2-7	X	High impedance	High impedance	Low	High impedance	Output high=! data
9	IC_2-8	X	High impedance	High impedance	High impedance	Low	Output high=! data

Modulating a reference allows maximum-value search for phase detection

Chien-Hung Chen, Hui-Shun Huang, Jyi-Jinn Chang, and Tai-Shan Liao,
National Applied Research Laboratories, Hsinchu, Taiwan

A lock-in amplifier is a useful tool for measuring a signal's amplitude and phase. A data-acquisition card can digitize the amplifier's output signal, and software can calculate amplitude and phase. A DSP or a general-purpose processor can also calculate amplitude and phase. The circuit in this Design Idea integrates two Analog Devices (www.analog.com) AD9954 DDS (direct digital synthesizers) and an AD630 balanced modulator/demodulator into a low-cost lock-in amplifier (**Figure 1**).

One AD9954 generates a reference signal and a measurement signal for the target. The AD630 then modulates the reference signal and the target signal. A lowpass filter removes the $2\omega t$ component that you calculate from the signal modulation. When the modulator function of the AD630 operates at frequencies higher than 50 kHz, however, the output waveform of the AD630 causes a measurement error and thus a signal-analysis error in the phase measurement.

When the reference and measurement signals are in phase, the result of

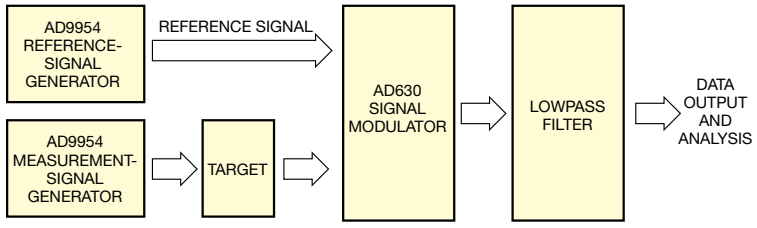


Figure 1 A lock-in amplifier comprises two signal generators, a modulator, and a lowpass filter.

modulation is at its maximum. A maximum-value-search method improves the operating frequency of the AD630's modulation function. Using a flow chart, you can control two AD9954s to generate the reference and target signals (**Figure 2**). The AD630 then modulates the two signals, digitizes the results, and stores them in registers. Later, you shift the phase of the reference signal and repeat the procedure until the circuit sweeps through all possible differences in phase.

You then search for the maximum value in the data set. When you modulate the signal at different phases, the phase shift of the reference signal indicates the phase shift of the target. **Table 1** represents the real case with 30° phase shift between the reference and the target signals. At 50 kHz, the error of lock-in calculation is 19%, which is larger than the 5% phase shift at 10 kHz. Those results indicate weak performance at high frequencies. Using the search results, you can increase the accuracy to 3% at 10 kHz and 7% at 50 kHz. EDN

TABLE 1 ERROR AS A FUNCTION OF FREQUENCY

Operation frequency (kHz)	Lock-in calculation error	Maximum-value-search error
1	29.669° (1%)	29.669° (1%)
10	28.451° (5%)	29.201° (2%)
50	24.275° (19%)	26.338° (12%)

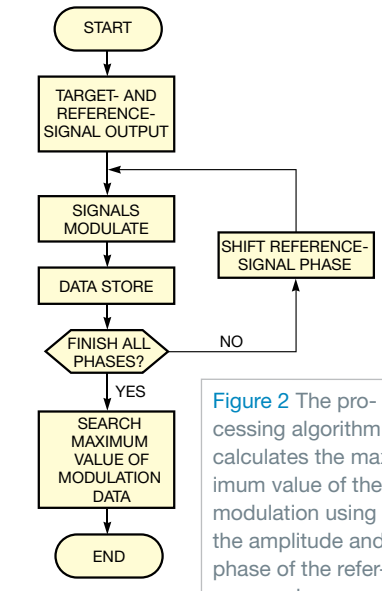


Figure 2 The processing algorithm calculates the maximum value of the modulation using the amplitude and phase of the reference and measurement signals.

Offline supply drives LEDs

TA Babu, Chennai, India

LEDs need power when rectified ac-mains voltage drops during its cycle. The circuit in **Figure 1** lets you use an inductor-less, switching, offline power supply as an LED driver for emergency-exit signs and neon-light replacements. The design uses off-the-shelf components, offers efficient operation without an inductor in the dc side of the circuit, has no high-voltage capacitors, operates directly from either 120 or 230V ac, has minimal power dissipation, and has adjustable output voltage.

The circuit operates by controlling the conduction angle of MOSFET Q_2. When the rectified ac voltage is below the high-voltage threshold, V_{TH}, which D_1 sets, the series pass transistor turns on. The series pass transistor turns off when the output storage capacitor, C_2, charges up to the regulation point.

The circuit's output voltage decays when Q_2 is off and when the rectified ac is below the output voltage (**Figure 2**). The load and the value of C_2 determine the amount of decay. The switch conducts only when it has low voltages across it, minimizing power dissipation.

The output capacitor charges on the rising edge of a sine wave, which achieves reasonable efficiencies. Fusible resistor R_1 provides catastrophic-failure protection and limits input inrush when you first apply ac power. A 15V diode, D_2, limits the voltage to the gate of Q_2 and limits the voltage across transistor Q_1.

The current interruption in the MOSFET causes ringing on the drain-to-source voltage of Q_2, creating conducted EMI (electromagnetic interference). The 2.2-mH choke, L_1, and capacitor C_1 suppress EMI. This design maintains a fairly constant illumination over

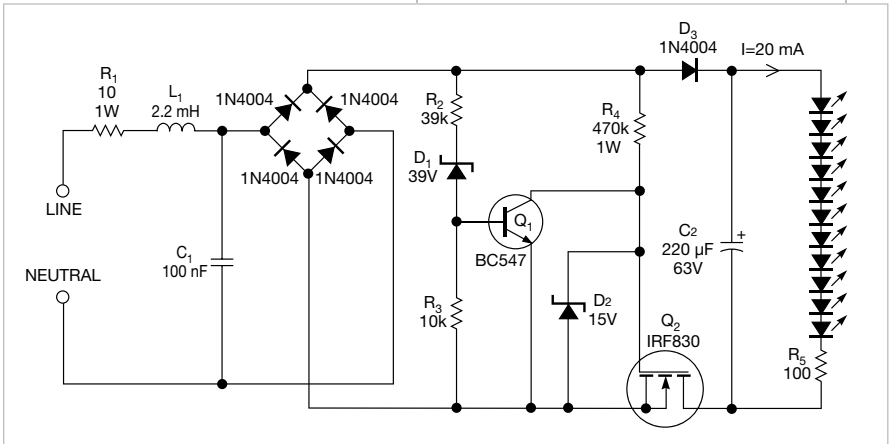


Figure 1 The transistor and MOSFET provide current to keep the LEDs lit.

a wide voltage variation in the input. If necessary, you can add a few more such strings to suit your requirements.

Note that this circuit does not provide galvanic isolation. Touching any part of the circuit during operation can give you an electric shock. EDN

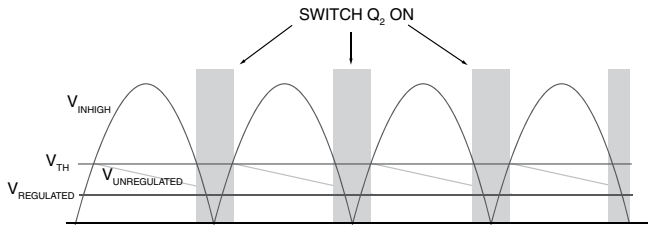


Figure 2 Switch Q_2 turns on when the rectified ac input voltage drops below a threshold.

Light an LED without wasting energy

Raju R Baddi, Tata Institute of Fundamental Research, Maharashtra, India

LEDs need current to illuminate, and current usually flows through a power supply to an LED. A typical LED-driver circuit uses a transistor to provide current and a series resistor to decrease the voltage you apply to the LED. Unfortunately, the energy $(V_{SOURCE}–V_{DIODE})×I_{DIODE}$ in a transistor/resistor combination goes to waste, giving off heat.

The circuit in **Figure 1** can minimize this waste by using an inductor and an oscillating circuit to control the current through the LED—energy that would otherwise go to waste. Inductor L_1 stores power and channels it back into the LED.

You might think to put two or more LEDs in series instead, but that configuration doesn't let you change the intensity and still save power. This circuit provides a general way of saving power without worrying about the intensity issues or operating voltage of the device. Transistors Q_1 and Q_2 alternately turn on and off. Q_1 increases the current through the LED from a certain minimum value when it connects the L_1/LED combination to a voltage source. Transistor Q_2 discharges stored energy in inductor L_1 through the LED. The current falls between a maximum and a minimum. Assume that transistors Q_1 and Q_2 are lossless switches in the analysis of this circuit.

Because the inductor doesn't let the current grow suddenly, it controls the average current through the LED to a desired value. The inductor also stores energy, which also powers the LED. You can obtain details, the average current through white LED D_3 as a function of inductance, and other parameters in the online version of this Design Idea at www.edn.com/110421dia. The following **equations**, which apply to the output of G_2, set the on- and off-times:

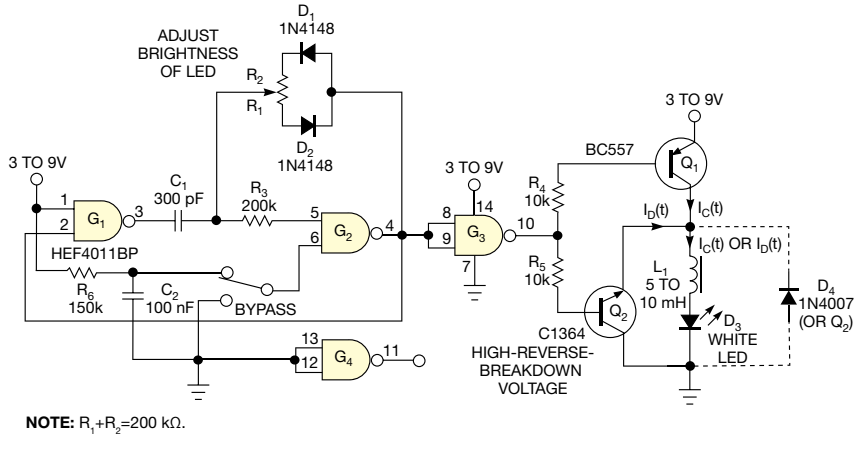
$$t_{OFF} \simeq R_1 C \ln\left(\frac{V+V_T-0.6}{V_T-0.6}\right);$$

$$t_{ON} \simeq R_2 C \ln\left(\frac{2V-V_T-0.6}{V-V_T-0.6}\right),$$

where V is the supply voltage and V_T is the input threshold voltage of the CMOS gates at supply-voltage V.

You can expect efficiencies as high as 80% with this circuit. Simulation results produce values of average current approximately the same as those in the Web version of this Design Idea. In this circuit, the supply current is less than the current through the LED because of the stored energy.

The current through the LED has a maximum and a minimum, which the on- and off-times of Q_1 and Q_2 set, along with other parameters, such as the value of L_1. You can use a 5- to 10-mH ferrite-core inductor for L_1 with a white LED with a forward-voltage drop of approximately 3V. For supply voltages of 7 to 15V, use a better transistor than Q_2, such as the 2SC3134, because of the reverse breakdown voltage of the base-emitter junction. The C1364 transistor in the **figure** works well at voltages as high as 9V. The **equations** apply to the CD4011BP, although you can substitute the HEF4011BP, which consumes less power. EDN



NOTE: $R_1+R_2=200$ kΩ.

Figure 1 This circuit lights an LED without wasting power when the source voltage is much higher than the LED's operating voltage.

productroundup

CIRCUIT PROTECTION

Electronic current limiters tolerate ac-mains-power contact

The TBU (transient-blocking-unit) DT-series circuit-protection devices tolerate ac-mains-power contact without circuit damage. The electronic current limiters provide protection against faults from short circuits, ac-power cross, induction, and lightning surges. The fast-reacting protectors do not alter the signal performance of high-speed communication ports, unlike high-capacitance protectors. The devices target use in outdoor applications, such as security systems, photovoltaic panels, and service kiosks. The series includes eight models offering continuous ac-voltage ratings as high as 425V rms and nominal trigger currents of 150 to 750 mA. The devices come in surface-mount DFN packages. The TBU-DT-065 and TBU-DT-085-XXX-WH sell for 69 cents each (15,000).
Bourns Inc, www.bourns.com

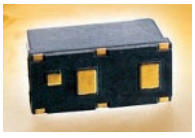
Transmitter/receiver switch delivers 260V p-p protection

The high-voltage, two-terminal, four-channel, bidirectional MD0105 voltage-protection device consumes 200 µA and protects the receiver circuitry of ultrasound systems from high-voltage transmitter pulses. A switch control that monitors the voltage drop across terminals A and B governs the normally closed MD0105 switch. The switch opens if the voltage difference exceeds ±2V. In the open state, 200 µA of current flows through the switch to determine whether high voltage is present. The switch does not close until the cross-terminal voltage drops below 2V. The IC replaces conventional discrete transmitter/receiver approaches and requires no diode bridges, inductors, resistors, or power rails. In an 18-lead DFN package, the MD0105K6-G sells for $3.58 (1000).

Supertex Inc, www.supertex.com

Thermal-protection devices save board space, assembly time

Designers can quickly and easily install the RTP (reflow-thermal-protection) series of surface-mount, ROHS-compliant devices using industry-standard pick-and-place and lead-free reflow equipment. The devices can withstand multiple reflow passes with peak temperatures exceeding 200°C; in the field, the devices open when they detect temperatures higher than 200°C. The RTP200 can replace redundant power FETs, relays, and heavy heat sinks that typically find use in automotive designs. The devices protect against thermal-runaway damage from capacitors, ICs, resistors, and other components that can crack and fail and against the effects of any type of corrosion-induced heating. They have a typical series resistance of 1.2 mΩ and high-current dc-interrupt ratings of 200A at 16V dc and 100A at 32V dc. The RTP200 sells for 48 cents each (10,000).



Tyco Electronics,
www.tycoelectronics.com

USB-OTG bus-port-protection array provides low typical capacitance

The VBUS053CZ-HAF ESD-protection array protects USB-OTG ports against transient-voltage signals. It has three lines of USB ESD protection at a 5.5V working range and one line of bus-voltage protection at a 28V working range. The device comes in a leadless LLP75-7L package with a profile of 0.6 mm and targets applications such as USB 2.0 and HDMI in HDTVs and mobile electronics. Load capacitance is 0.7 pF for the three data lines—D+, D−, and ID—and maximum leakage current is 0.085 µA at a working voltage of 3.3V and 1 µA at a working voltage of 5.5V. The array provides a typical clamping voltage of 53V at 3A and sells for $15 (100).

Vishay Intertechnology,
www.vishay.com

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This advertising is for new and current products.

Floats like a butterfly, stings like a bee

In the early 1990s, I was the product-engineering manager for a small semiconductor company making clock-generator ICs. Our group was responsible for checking out the first silicon on new designs to make sure they functioned and performed correctly. We introduced a new version that had only some minor changes on an established and well-characterized design, so I left the initial checkout in the capable hands of our summer intern.

I didn't have to wait long before there was a call from the lab. "The part works perfectly the first time it's powered up, but not the second time," the intern said.

When I got to the lab, the responsible design engineers were there. After zapping a few more parts, just to be sure they truly had all died, we began to list all the potential causes we could think of. Was the part latching up due to a parasitic SCR (silicon-controlled rectifier)? Was there a layout error? Someone ran off to redo the LVS (layout-versus-schematic) check and DRCs (design-rule checks). Had we bonded the pins correctly? Someone took a sample for decapsulation and comparison with the bond diagram. Were there problems at the wafer fab? We looked at the electrical-test data from the wafer fab and found no hint of anything amiss. The design engineers went back to their workstations to recheck the design, and I sat down at the bench for some serious troubleshooting.

My favorite hypothesis was that there was a floating node somewhere on the chip. Etching problems in the fab can cause bad connections between metal and silicon or between metal layers, and these bad connections can cause floating nodes. Sometimes, designers just plain forget to hook things up.

A floating node also fit the observed phenomena. Maybe the node could charge to one logic level on the initial power-up and to the other on subsequent power-ups. If the floating node controlled an enable or power-down line, that fact could explain why the part worked only the first time we powered it up. We set some failing devices aside to see whether they would recover in a few hours.

A floating node might charge differently if we slowly ramped the power supply up and down. Sure enough, if I turned the power to the chip on and off by using the voltage-adjustment knob on the bench supply, it would survive through multiple power cycles.

IT WAS ZAPPING ALL THE PARTS AT THE END OF THEIR FIRST POWER CYCLE, SO THEY NEVER WORKED AGAIN.

"Just how fast are these supplies?" I wondered. We had recently purchased some new technology, our first DSO (digital storage oscilloscope), so I hooked it up to find out. We turned on the supply, and the captured trace was entirely unremarkable—a well-behaved smooth ramp to 5V in 100 msec.

I reached over to turn off the supply, and, as I did, the scope triggered again. There on the screen was the cause of our problems. When I turned off the supply, it briefly soared to 20V before heading to 0V. It was zapping all the parts at the end of their first power cycle, so of course they never worked again. We tried another bench supply, and the part worked fine through multiple power cycles.

Word quickly spread through the building that there was nothing at all wrong with our new part. We quickly tested samples and sent them out to customers. And the defective power supply? We taped a printout of that ugly power-off characteristic to it and sent it in for warranty repair. Its manufacturer replaced it with a new one—no questions asked. EDN

Jan Gazda is an engineer in Issaquah, WA. You can reach him at gazda.jan@live.com.

www.edn.com/tales

DANIEL VASCONCELLOS

Making security the foundation of functionality.

"AES-NI boosts AES encryption by 3x and decryption over 10x compared to pure software implementations of OpenSSL."

Praveen Mosur
Network Security Architect
Intel® Embedded and Communications Group

CHALLENGE >>>

How to keep embedded devices secure without sacrificing performance?

From transportation to medical devices to automated factory systems, the number of embedded devices is growing exponentially. And so are the corresponding security threats. We now live in a world with a few billion smart, connected devices and over 60,000 new malware signatures identified each day.[1]

SOLUTION >>>

Move from a "known bad" to a "known good" model of security.

Instead of simply reacting to known bad signatures, wouldn't it be better to proactively shift embedded security to a "known good" model? One where you can trust the device you are communicating with? As the embedded universe continues to expand, achieving this new paradigm begins with three key elements.

Authentication

Quickly verifying a good signature instead of filtering bad ones means more resources can be devoted to focusing on the device's intended task. Which is why Intel created a true Random Number Generator that produces unpredictable random keys to help verify trusted connections.

Device Integrity

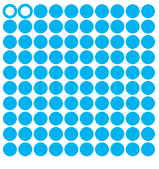
If your hardware isn't secured, the solution on top of it can't be trusted. A combination of Intel® Virtualization Technology and Intel® Trusted Execution Technology enables a root of trust in hardware and secure isolation of critical code and data.

Data Protection

We need to ensure that data gets to its destination uncompromised. To make powerful encryption easier, we are adding AES new instructions (AES-NI) to our processors for up to 10-times faster crypto processing, without impacting application performance and functionality.

Intel believes that security goes hand-in-hand with functionality. Which is why we're continually working on new ways to provide you with proactive security building blocks that hit the performance, power, and cost targets you expect today, with the flexible scalability you'll need for tomorrow.

75 percent of enterprises surveyed by Symantec experienced some form of cyber attack in 2009.[2]



Threats to confidential information that incorporated remote access capabilities grew to 98 percent in 2009.[3]

Across embedded, new ideas and solutions to address security are continually emerging. From implementing secure end-to-end systems to protecting personal data to other security innovations, keep up with the critical information that is shaping the embedded landscape.

READ > WATCH > DISCUSS >>> **intel.com/embedded/innovation/security**

 [1] McAfee Threats Report, Third Quarter 2010. [2] Symantec State of Enterprise Security Report 2010. [3] Symantec Global Internet Security Threat Report 2010.

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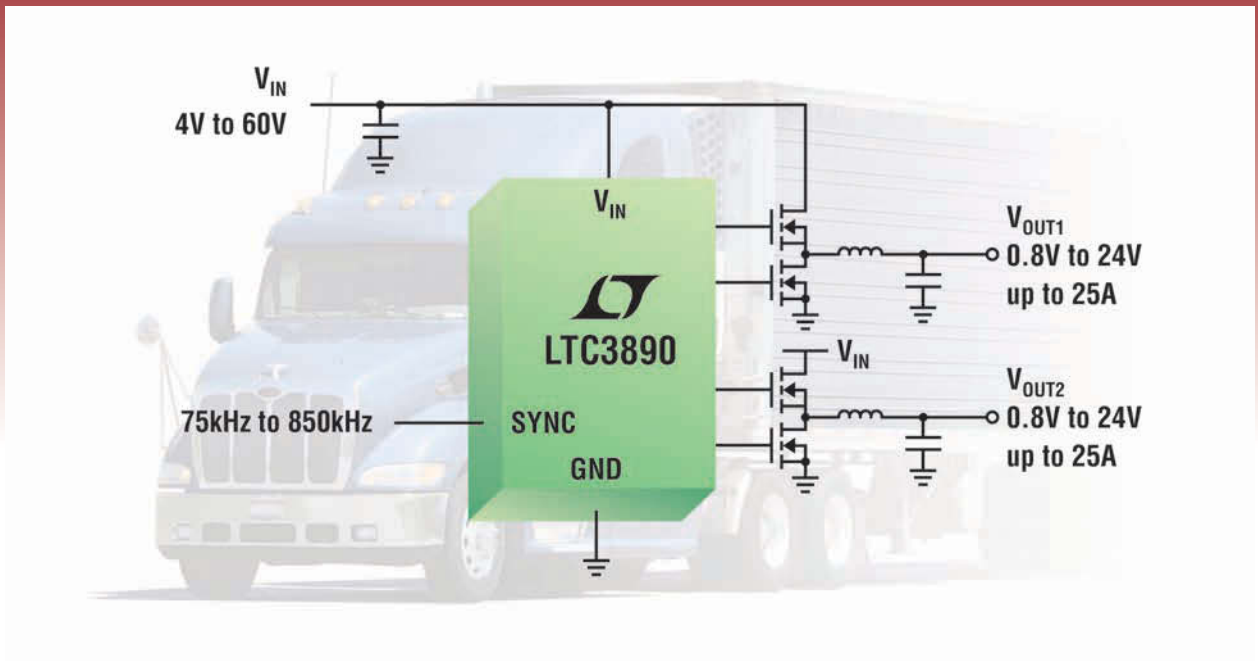
All the Highs & a Low



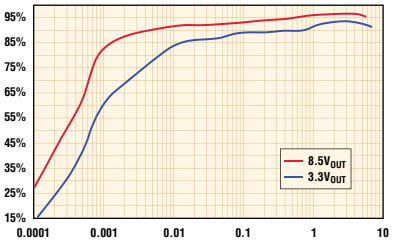
$60V_{IN}$, $24V_{OUT}$, 25A/Channel, 850kHz & I_Q = 50µA

A new generation of dual synchronous, micropower step-down controller, the LTC®3890 offers performance and feature advantages for a broad range of power conversion applications. The 4V to 60V input capability covers a wide range of input sources and battery chemistries, protecting against high voltage transients so surge suppression circuits are not required. Minimum on-time of 95ns enables high step-down ratios. Its powerful 1.1Ω onboard N-channel MOSFET drivers can deliver up to 25A of continuous output current per channel.

Features

- Input Voltage Range: 4V to 60V
- Dual Output Voltages: Up to 24V
- Up to 25A Output per Channel
- 95% Efficient
- Low Quiescent Current: 50µA
- Multiphase Capable for Higher Output Current & Low Input Ripple
- High Step-Down Ratios
- R_{SENSE} or Inductor DCR Sensing
- Single Output Version: LTC3891

Efficiency vs Output Current (A)



V_{IN} = 24V, F_{SW} = 225kHz

Info & Free Samples

www.linear.com/3890

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www.linear.com/ad/3890

LINEAR TECHNOLOGY